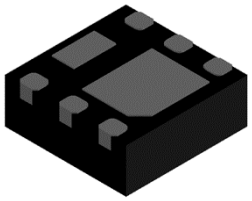
SNM046R8DA

Single N-Channel, 40V, 18.2A, Power MOSFET

http://www.sitcores.com/

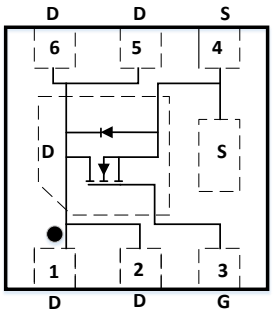
V_{DS} (V)	Max.$R_{DS(on)}$ (mΩ)
40	6.8 @ V_{GS}=10V
	10.6 @ V_{GS}=4.5V



DFN2X2-6L

Description

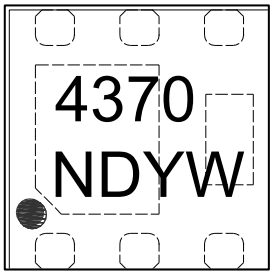
The SNM046R8DA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM046R8DA is in compliance with RoHS.



Pin configuration (Top view)

Features

- Trench Technology
- Supper high density cell design
- Low ON resistance
- Package DFN2X2-6L



4370 =Device Code
DN =Special Code
Y =Year
W =Week (A~z)

Marking

Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
SNM046R8DA-6/TR	DFN2x2-6L	3000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current [e]	T_A=25°C	I_D	18.2	A
	T_A=100°C		14.6	
Pulsed Drain Current [c]		I_{DM}	122	A
Avalanche Energy L=0.3mH		E_{AS}	41	mJ
Power Dissipation [a]	T_A=25°C	P_D	3.8	W
	T_A=70°C		2.4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	25	32.5	°C/W
	Steady State		52	65	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm2 area)

b Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

c The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

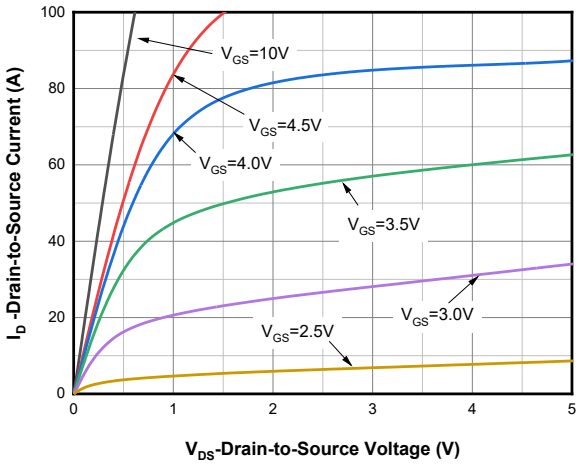
d The parameter is not subject to production test – verified by design / characterization.

e The power dissipation PD is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150°C.

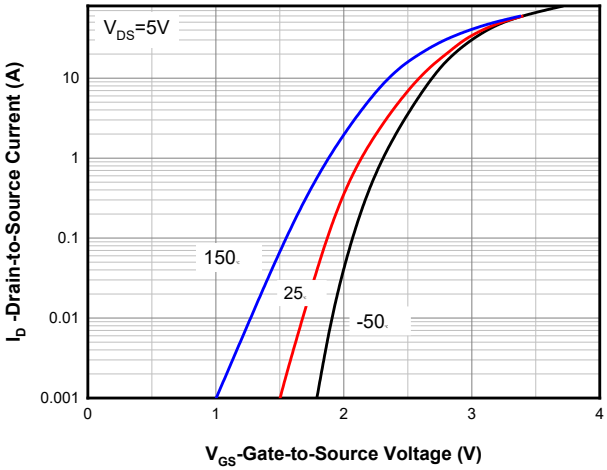
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V			1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	1.3	1.7	2.1	V
Drain-to-source On-resistance [c]	$R_{DS(on)}$	V_{GS} =10V, I_D = 10A		5.6	6.8	mΩ
		V_{GS} =4.5V, I_D = 10A		8.2	10.6	mΩ
CHARGES, CAPACITANCES AND GATE RESISTANCE[d]						
Input Capacitance	C_{ISS}	V_{GS} = 0V, f = 1.0MHz, V_{DS} = 25V		919		pF
Output Capacitance	C_{OSS}			212		
Reverse Transfer Capacitance	C_{RSS}			12.0		
Total Gate Charge（V_{GS}=10V）	$Q_{G(TOT)}$	V_{GS} =10V, V_{DS} = 20V, I_D = 10 A		11.8		nC
Total Gate Charge（V_{GS}=4.5V）	$Q_{G(TOT)}$			5.6		
Gate-to-Source Charge	Q_{GS}			2.7		
Gate-to-Drain Charge	Q_{GD}			1.5		
Gate Resistance	R_g	f=1MHz		1.4		Ω
SWITCHING CHARACTERISTICS [d]						
Turn-On Delay Time	td(ON)	V_{GS} = 10 V, V_{DS} = 32 V, R_G=5 Ω, I_D=10 A		5.8		ns
Rise Time	tr			2.8		
Turn-Off Delay Time	td(OFF)			17.6		
Fall Time	tf			4.0		
BODY DIODE CHARACTERISTICS						
Forward Voltage [c]	V_{SD}	V_{GS} = 0 V, I_S = 10A		0.85	1.2	V
Reverse Recovery Time	T_{rr}	I_F=10A, di/dt=100A/us		19.8		ns
Reverse Recovery Charge	Q_{rr}			7.7		nC

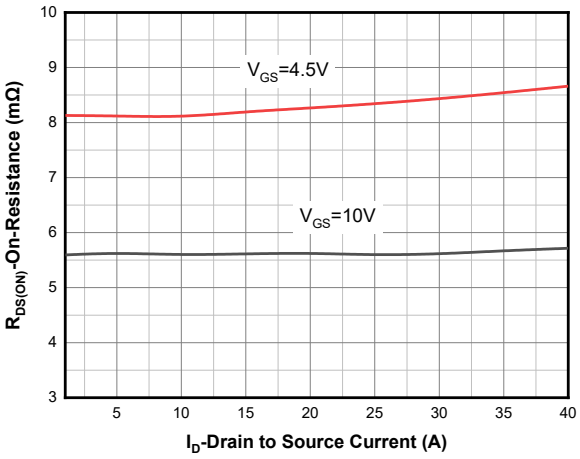
Typical Characteristics (Ta=25°C, unless otherwise noted)



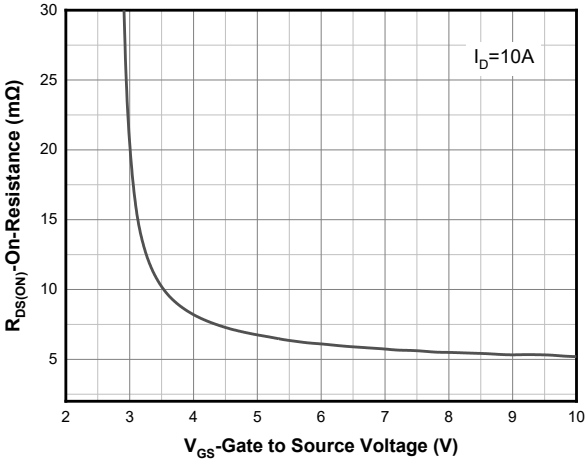
Output Characteristics [C]



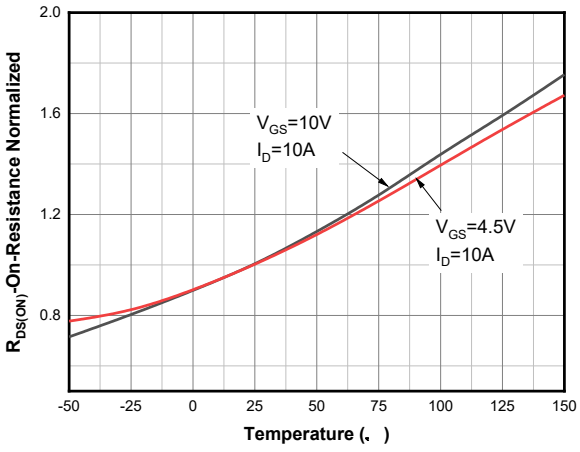
Transfer Characteristics [C]



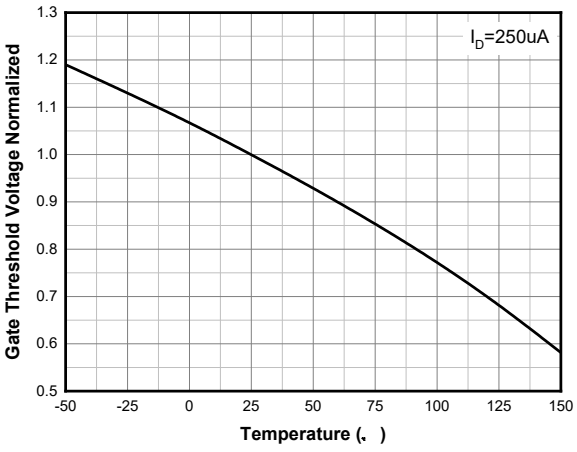
On-Resistance vs. Drain Current [C]



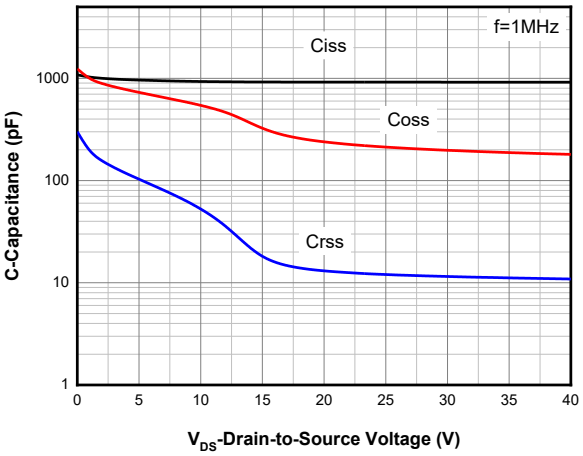
On-Resistance vs. Gate-to-Source Voltage[C]



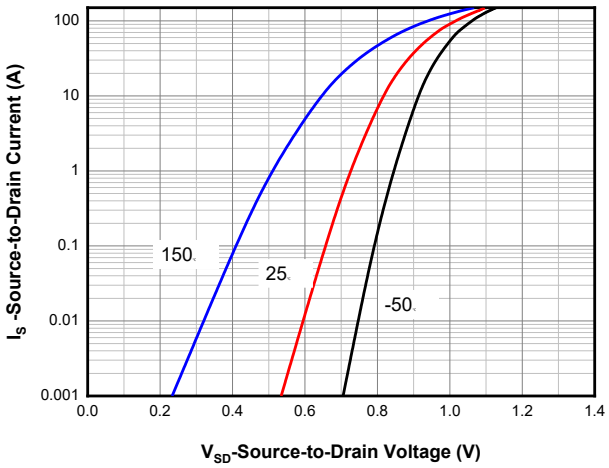
On-Resistance vs. Junction Temperature [C]



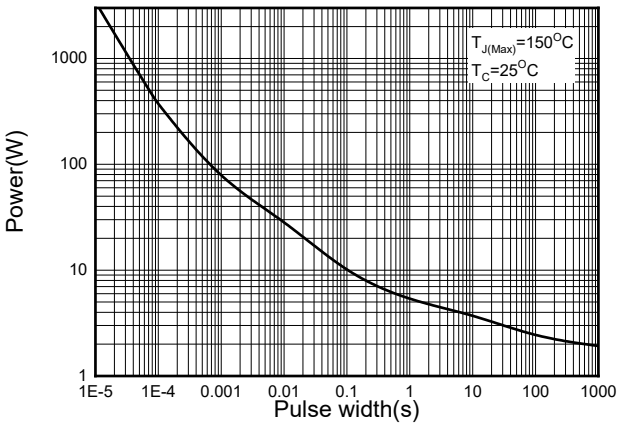
Threshold Voltage vs. Temperature



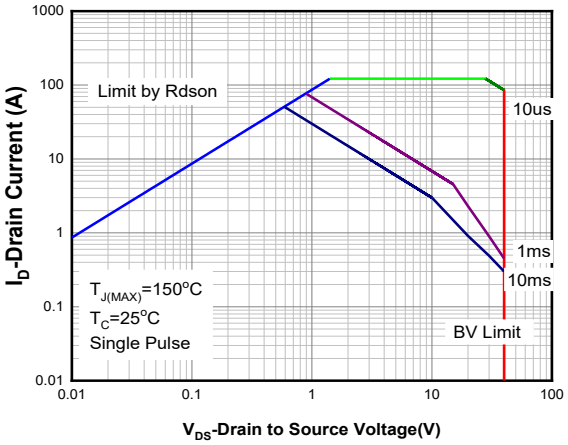
Capacitance



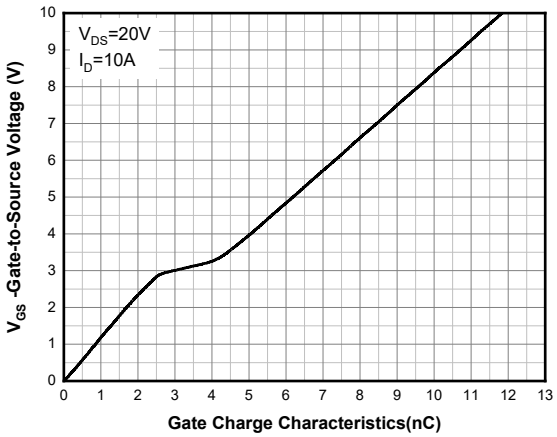
Body Diode Forward Voltage [C]



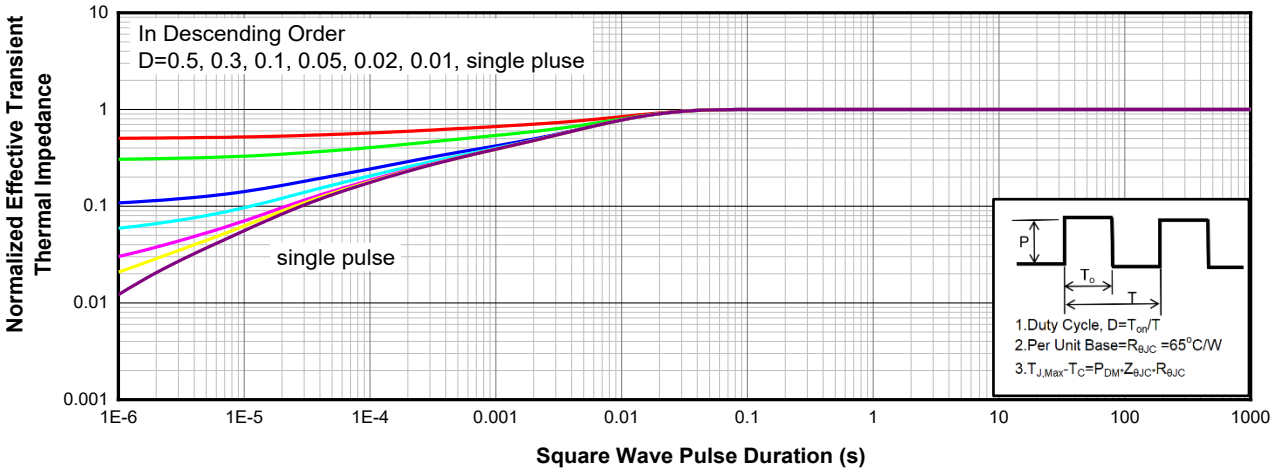
Single Pulse power



Safe Operating Area



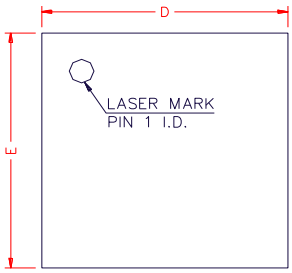
Gate Charge Characteristics



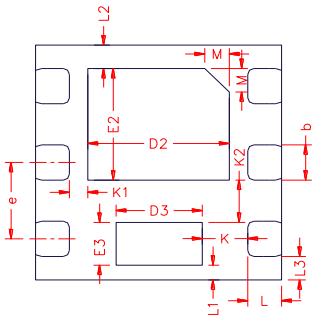
Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

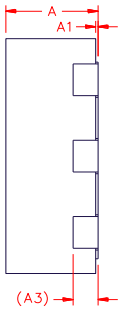
DFN2x2-6L



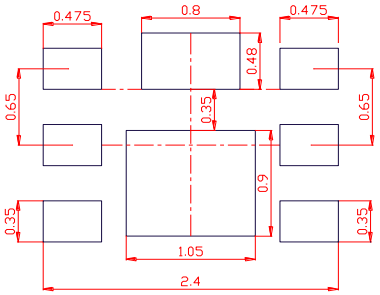
TOP VIEW



BOMTTOM VIEW



SIDE VIEW

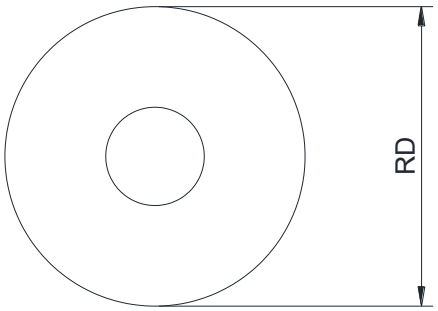


RECOMMENDED LAND PATTERN(unit： mm)

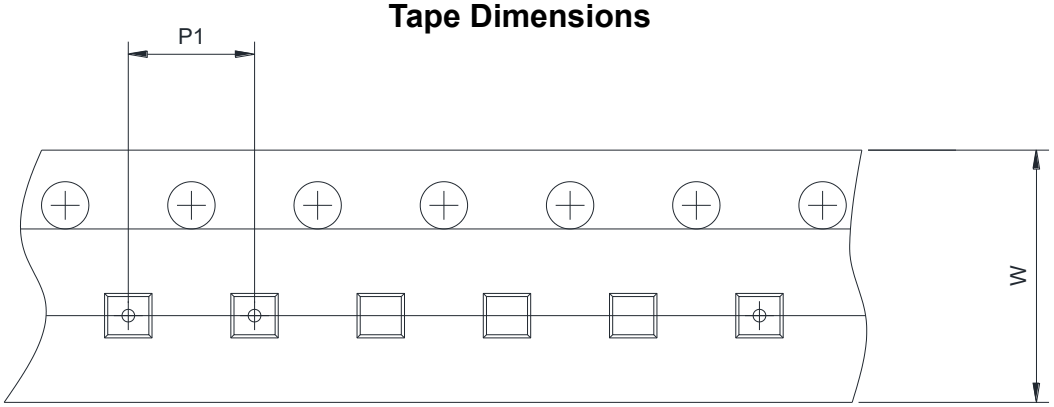
Symbol	Dimensions in Millimeters		
	Min.	Nom	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.25	0.30	0.35
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D2	1.05	1.15	1.25
E2	0.85	0.95	1.05
D3	0.60	0.70	0.80
E3	0.265	0.365	0.465
e	0.55	0.65	0.75
K		0.37Ref	
K1		0.15Ref	
K2		0.36Ref	
L	0.225	0.275	0.325
L1		0.125Ref	
L2, L3, M		0.20Ref	

TAPE AND REEL INFORMATION

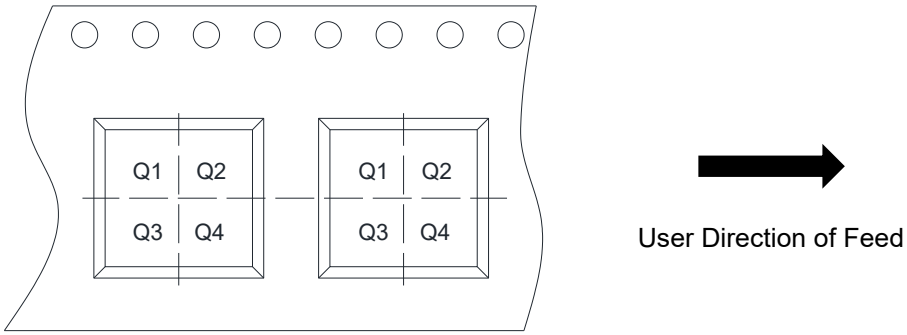
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4