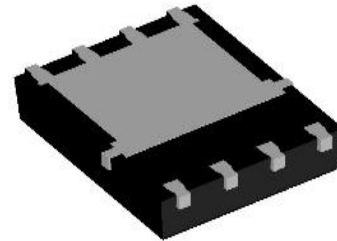


SNM037R0DNA

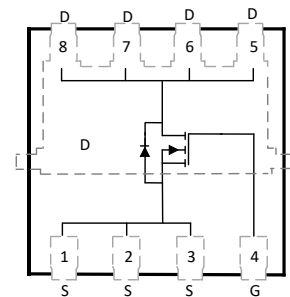
Single N-Channel, 30V, 48A, Power MOSFET

<http://www.sitcores.com/>

V_{DS} (V)	Max. $R_{DS(on)}$ (m Ω)
30	7.0 @ $V_{GS}=10V$
	11.5 @ $V_{GS}=4.5V$



PDFN5X6-8L



Pin configuration (Top view)

Description

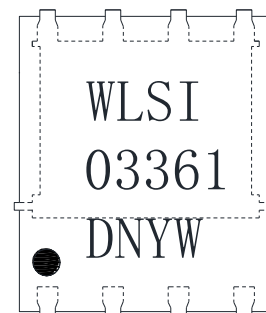
The SNM037R0DNA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced Split Gate Trench and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM037R0DNA is Pb-free.

Features

- Split Gate Trench Technology
- Supper high density cell design
- Low ON resistance
- Package PDFN5X6-8L
- 100% UIS and RG Tested
- MSL3

Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device



WLSI = Company (Group) Code
 03361 =Device Code
 DN =Special Code
 Y =Year
 W =Week(A~z)
Marking

Order information

Device	Package	Shipping
SNM037R0DNA-8/TR	PDFN5X6-8L	5000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_C=25^{\circ}\text{C}$	I_D	48	A
	$T_C=100^{\circ}\text{C}$		30	A
Pulsed Drain Current ^c		I_{DM}	136	A
Continuous Drain Current	$T_A=25^{\circ}\text{C}$	I_{DSM}	23	A
	$T_A=70^{\circ}\text{C}$		18	
Avalanche Energy $L=0.3\text{mH}$		E_{AS}	28	mJ
Power Dissipation ^b	$T_C=25^{\circ}\text{C}$	P_D	26	W
	$T_C=100^{\circ}\text{C}$		10	
Power Dissipation ^a	$T_A=25^{\circ}\text{C}$	P_{DSM}	5.9	W
	$T_A=70^{\circ}\text{C}$		3.8	
Operating Junction Temperature		T_J	-55 to 150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 to 150	$^{\circ}\text{C}$

Thermal resistance ratings

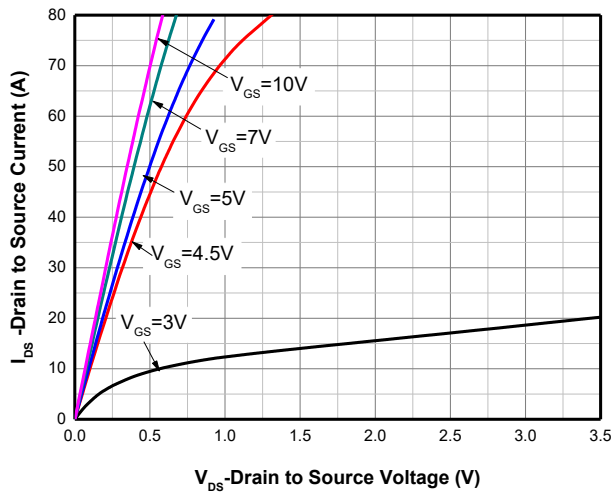
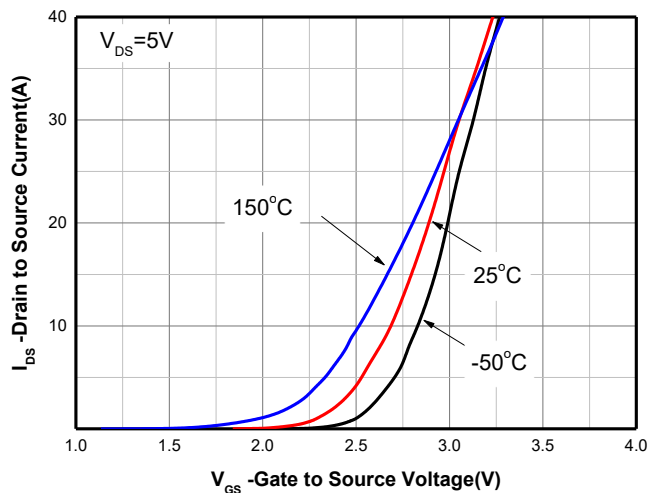
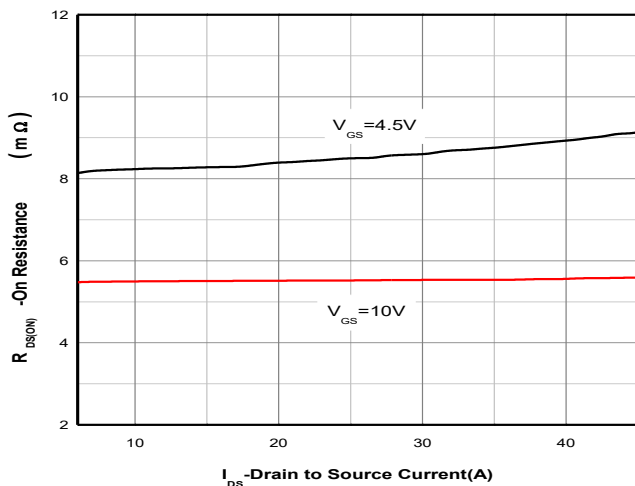
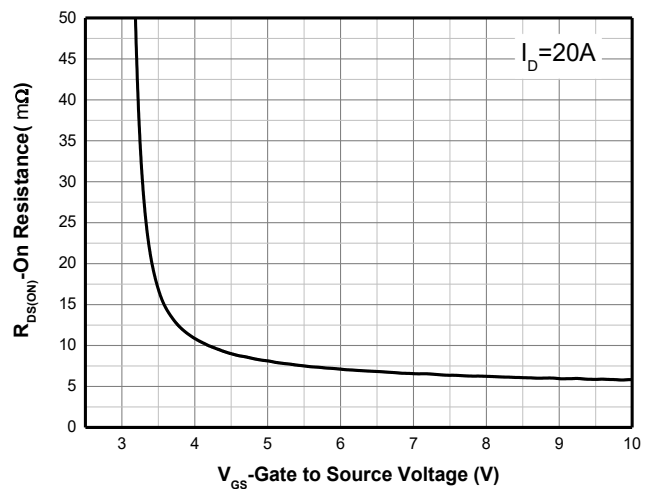
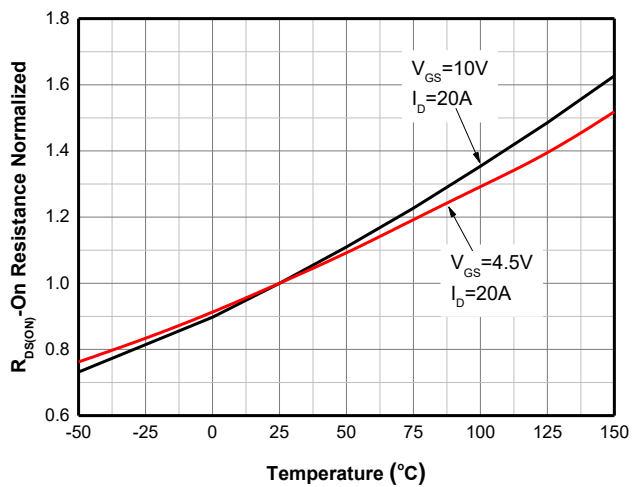
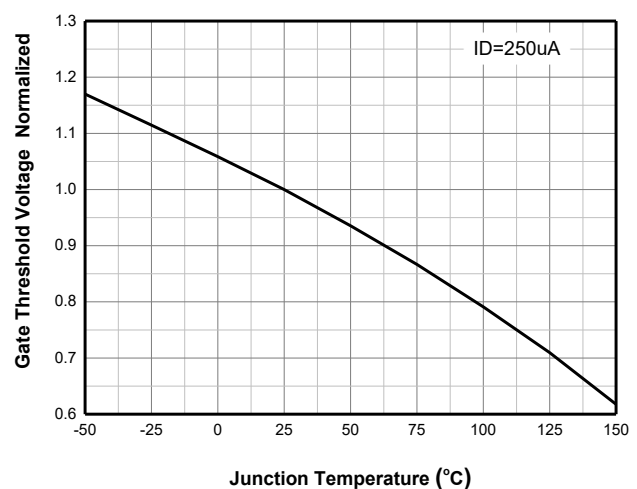
Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ^a	$t \leq 10\text{ s}$	$R_{\theta JA}$	17.0	21.2	$^{\circ}\text{C/W}$
	Steady State		40.3	50.4	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	3.9	4.8	

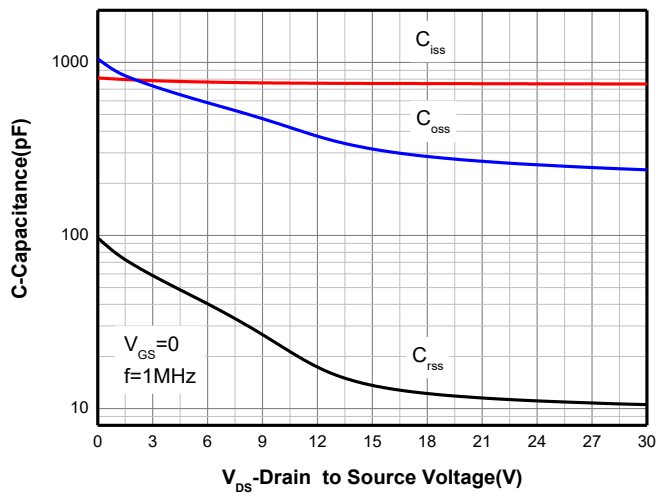
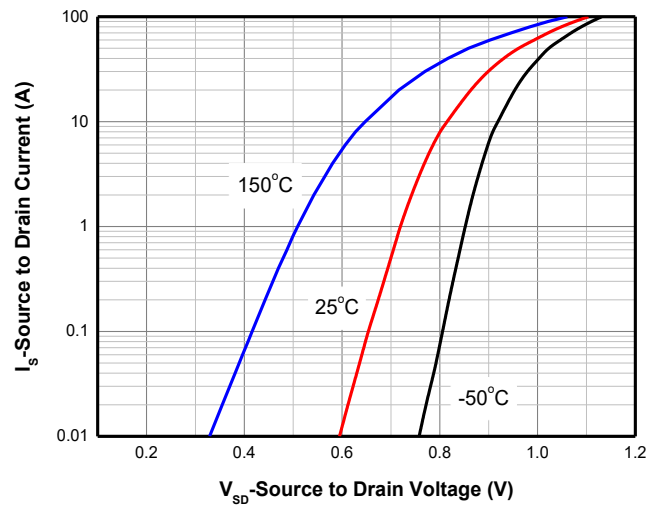
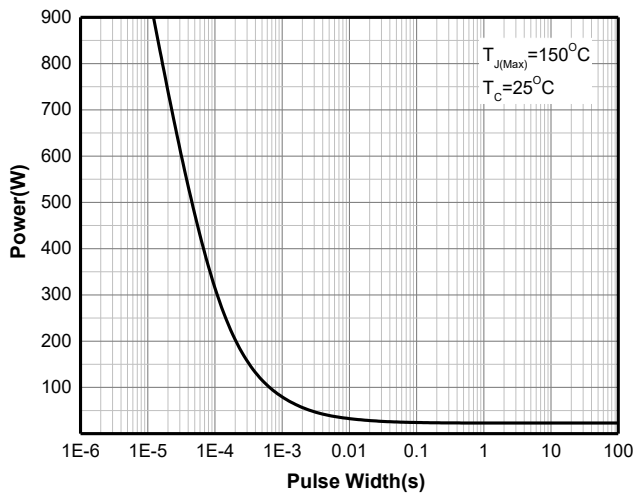
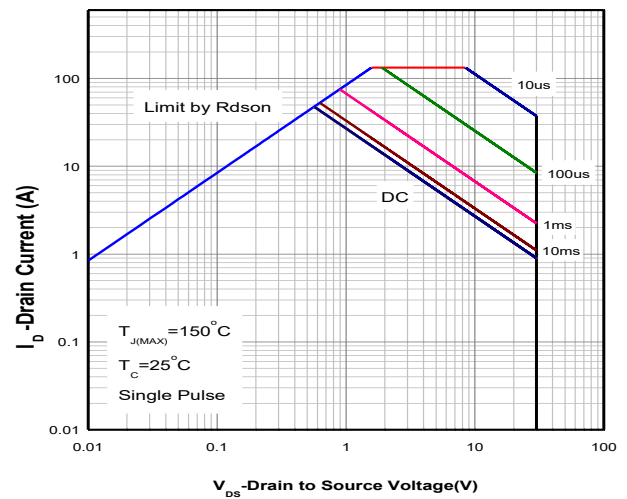
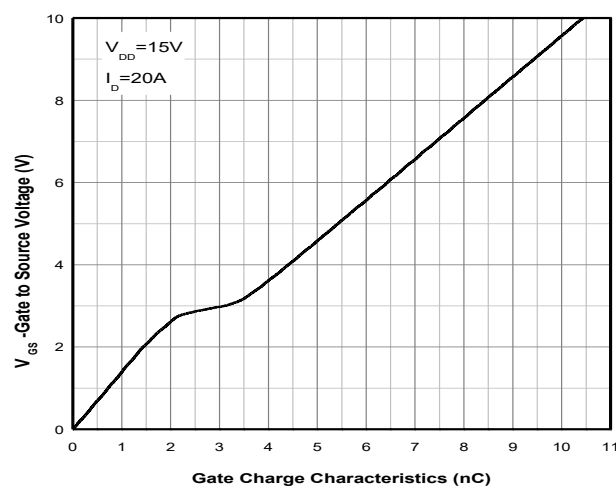
Note:

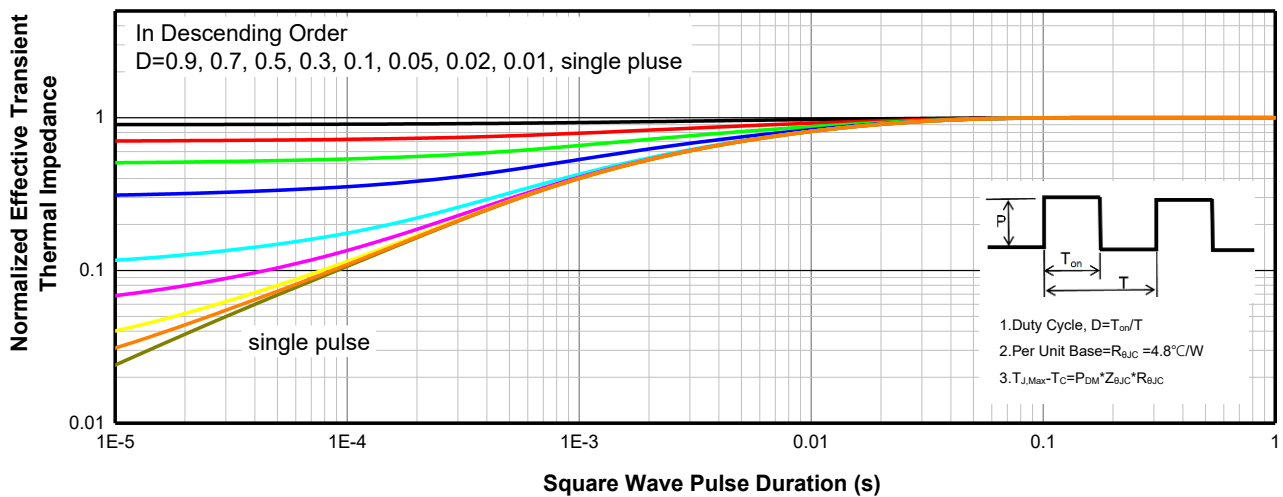
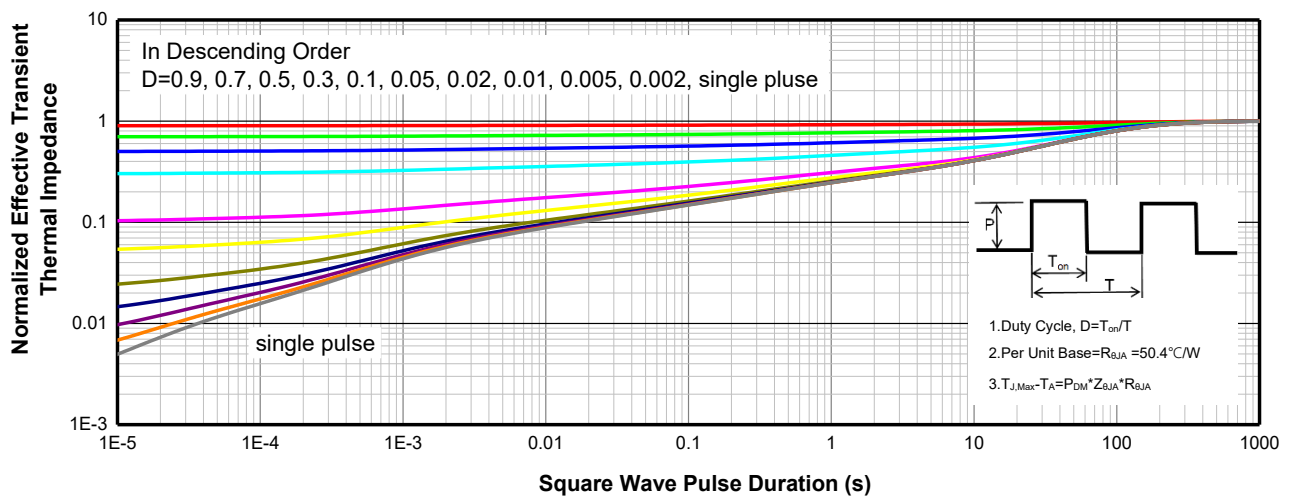
- a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm² area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ $t \leq 10\text{s}$ value and the $T_{J(MAX)}=150^{\circ}\text{C}$. The value is only for reference, any application depends on the user's specific board design.
- b The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial $T_J = 25^{\circ}\text{C}$, the maximum allowed junction temperature of 150°C .
- d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.
- e The parameter is not subject to production test – verified by design / characterization.

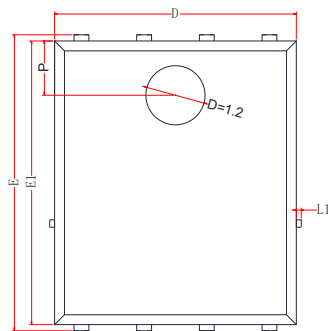
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250uA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	μA
Gate-to-source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250uA	1.1	1.6	2.1	V
Drain-to-source On-resistance ^d	R _{DS(on)}	V _{GS} =10V, I _D = 20A		5.5	7.0	mΩ
		V _{GS} = 4.5V, I _D = 20A		8.4	11.5	
CHARGES, CAPACITANCES AND GATE RESISTANCE ^e						
Input Capacitance	C _{ISS}	V _{GS} = 0V, f = 1.0MHz, V _{DS} = 15 V		734		pF
Output Capacitance	C _{OSS}			515		
Reverse Transfer Capacitance	C _{RSS}			18		
Total Gate Charge	Q _{G(10V)}	V _{GS} = 10 V, V _{DD} = 15V, I _D = 20A		10.4		nC
Total Gate Charge	Q _{G(4.5V)}			4.8		
Gate-to-Source Charge	Q _{GS}			2.2		
Gate-to-Drain Charge	Q _{GD}			1.2		
Gate Resistance	R _g	F = 1MHz		2.0		Ω
SWITCHING CHARACTERISTICS ^e						
Turn-On Delay Time	td(ON)	V _{GS} = 10 V, V _{DD} = 15 V, I _D = 20A , R _G = 3Ω		3.7		ns
Rise Time	tr			53.5		
Turn-Off Delay Time	td(OFF)			8.8		
Fall Time	tf			12.1		
Body Diode Reverse Recovery Time	t _{rr}	I _F =20A,di/dt=100A/us		22.5		ns
Body Diode Reverse Recovery Charge	Q _{rr}	I _F =20A,di/dt=100A/us		11.0		nC
BODY DIODE CHARACTERISTICS						
Forward Voltage ^d	V _{SD}	V _{GS} = 0 V, I _S = 1A		0.7	1.2	V
Maximum Continuous Current	I _S				26	A

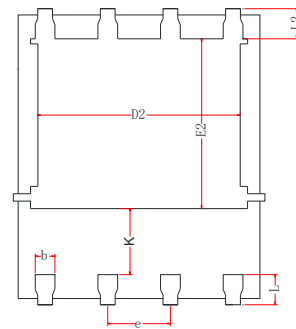
Typical Characteristics (Ta=25°C, unless otherwise noted)

Output Characteristics^d

Transfer Characteristics^d

On-Resistance vs. Drain Current^d

On-Resistance vs. Gate-to-Source Voltage^d

On-Resistance vs. Junction Temperature^d

Threshold Voltage vs. Temperature


Capacitance

Body Diode Forward Voltage^d

Single Pulse power

Safe Operating Area

Gate Charge Characteristics

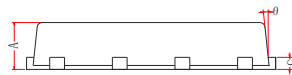

Transient Thermal Response (Junction-to-Case)

Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS
PDFN5x6-8L


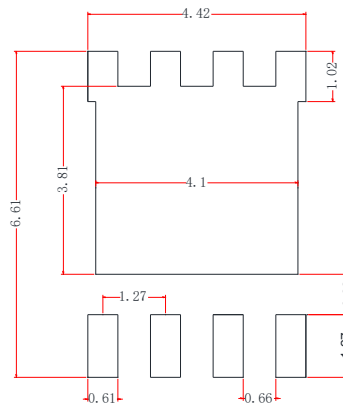
TOP VIEW



BOTTOM VIEW

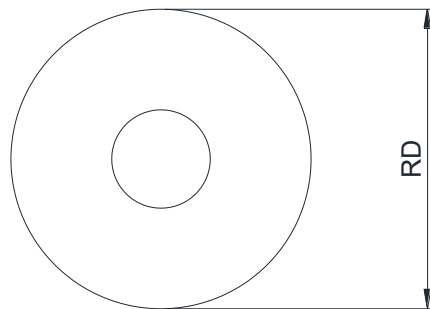
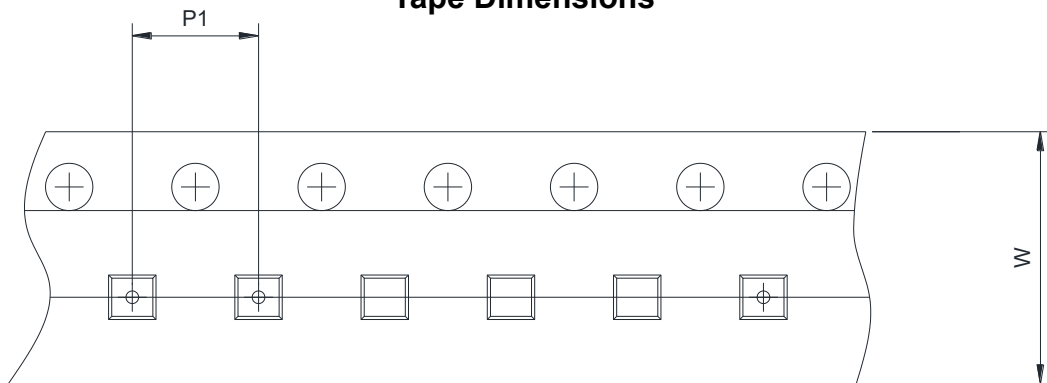
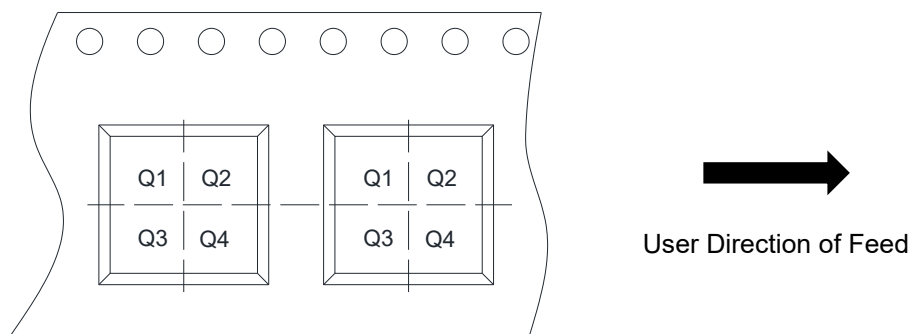


SIDE VIEW



RECOMMENDED LAND PATTERN (Unit:mm)

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	1.00	1.10	1.20
b	0.35	0.40	0.45
c	0.21	0.25	0.34
D	4.80	4.90	5.00
D2	3.82	-	4.11
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.18	-	3.54
e	1.27BSC		
K	1.10	-	-
L	0.51	0.61	0.71
L1	-	-	0.10
L2	0.51	0.61	0.71
P	1.00	1.10	1.20
θ	8°	-	12°

TAPE AND REEL INFORMATION
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


RD	Reel Dimension	☐ 7inch	☒ 13inch
W	Overall width of the carrier tape	☐ 8mm	☒ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm ☒ 8mm
Pin1	Pin1 Quadrant	☒ Q1	☐ Q2 ☐ Q3 ☐ Q4