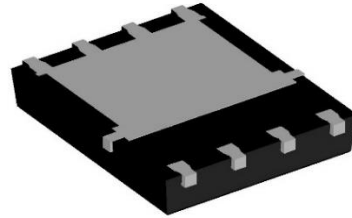
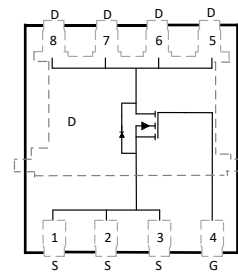


SNM033R4DNA
Single N-Channel, 30V, 89A Power MOSFET

V_{DS} (V)	Max. $R_{DS(on)}$ (m Ω)
30	3.4 @ $V_{GS}=10V$
	5.5 @ $V_{GS}=4.5V$

<http://www.sitcores.com/>

Descriptions

The SNM033R4DNA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM033R4DNA is Pb-free.

PDFN5X6-8L

Pin configuration (Top view)

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Extremely Low Threshold Voltage
- Package PDFN5X6-8L
- 100% Rg and Avalanche Tested
- MSL3

WLSI	=Company (Group) Code
03330	=Device Code
DN	= Special Code
Y	=Year
W	=Week(A~z)

Marking
Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
SNM033R4DNA-8/TR	PDFN5X6-8L	5000/Tape&Reel

Absolute Maximum ratings

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^d	I_D	$T_C=25^\circ\text{C}$	89
		$T_C=100^\circ\text{C}$	57
Pulsed Drain Current ^c	I_{DM}	235	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	35
		$T_A=70^\circ\text{C}$	28
Avalanche Energy $L=0.3\text{mH}$	E_{AS}	65	mJ
Power Dissipation ^b	P_D	$T_C=25^\circ\text{C}$	43
		$T_C=100^\circ\text{C}$	17
Power Dissipation ^a	P_{DSM}	$T_A=25^\circ\text{C}$	6.8
		$T_A=70^\circ\text{C}$	4.3
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal resistance ratings

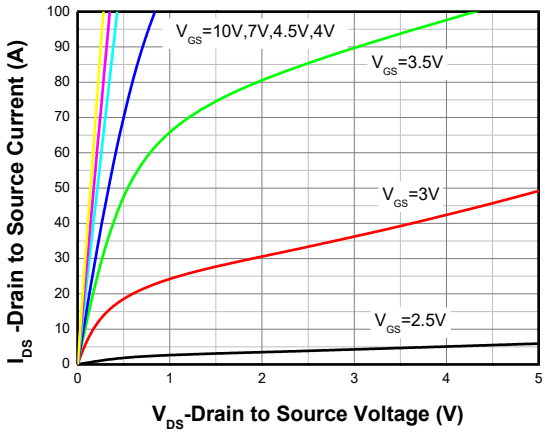
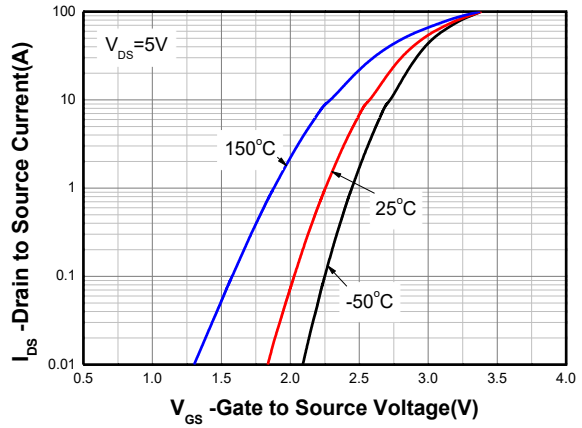
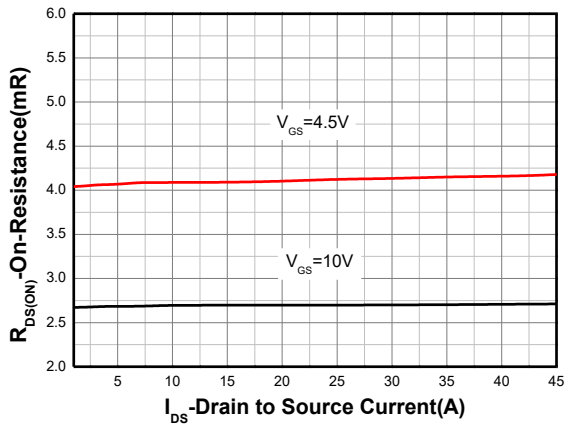
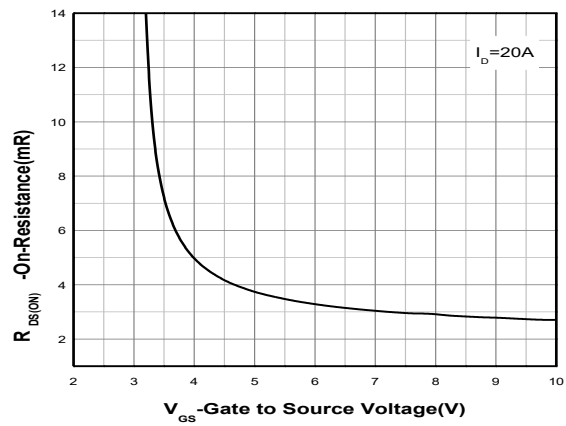
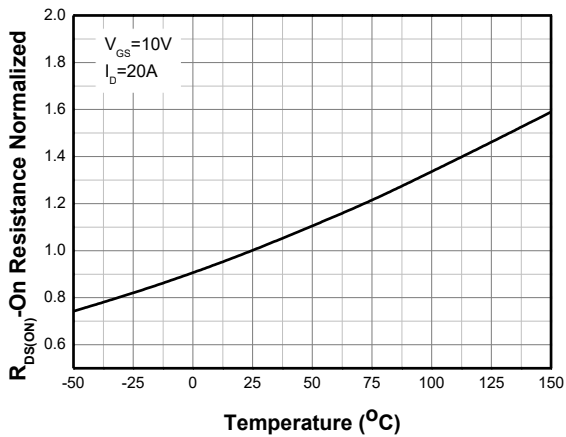
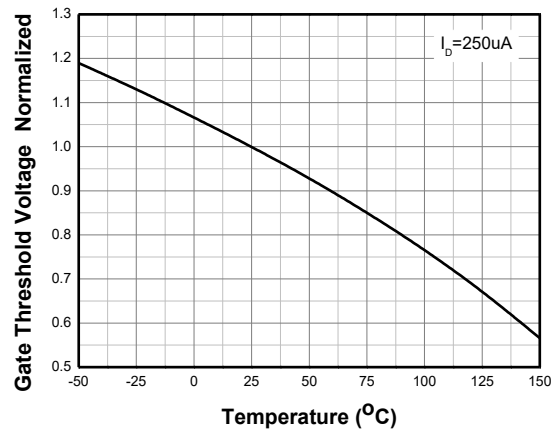
Single Operation					
Parameter	Symbol	Typical	Maximum	Unit	
Junction-to-Ambient Thermal Resistance ^a	$R_{\theta JA}$	$t \leq 10\text{ s}$	14.5	18.5	$^\circ\text{C/W}$
		Steady State	41.5	51.5	
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	2.3	2.9		

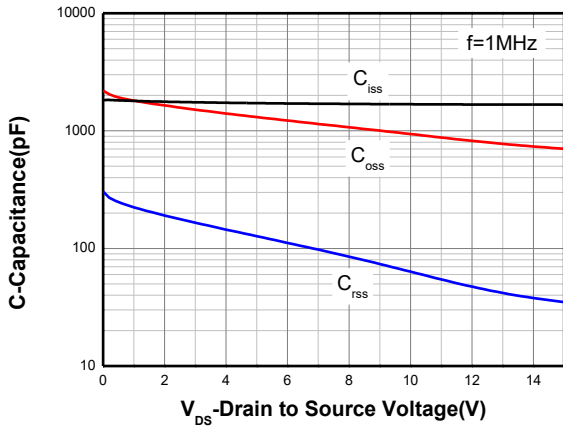
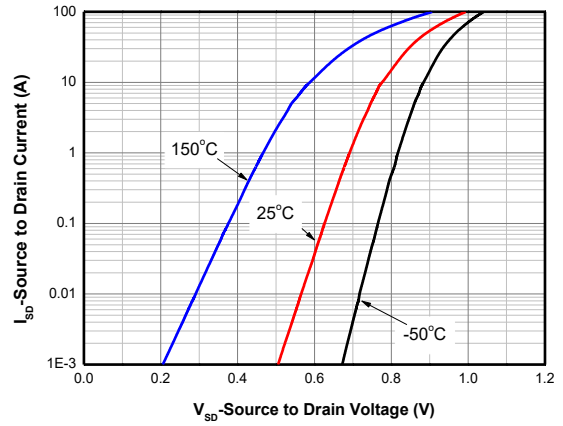
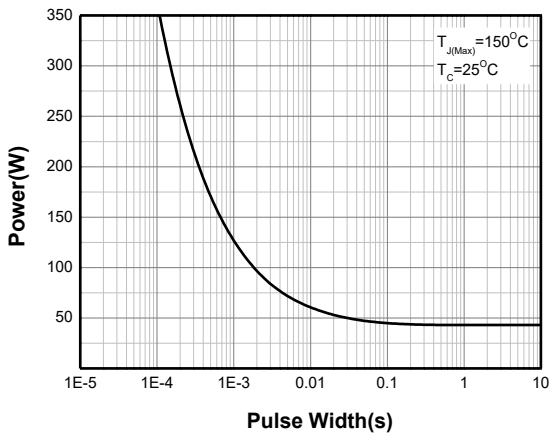
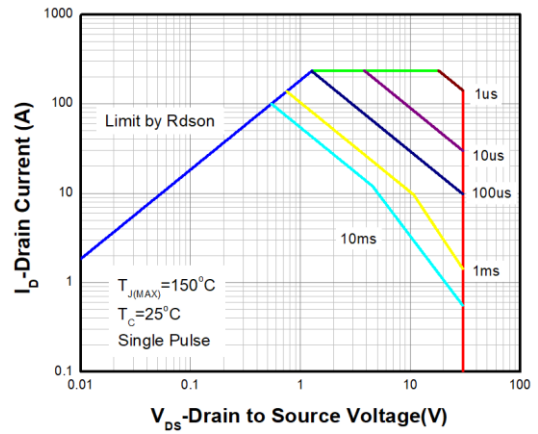
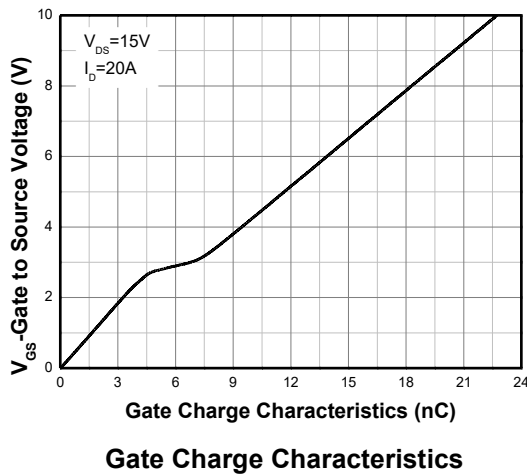
Note:

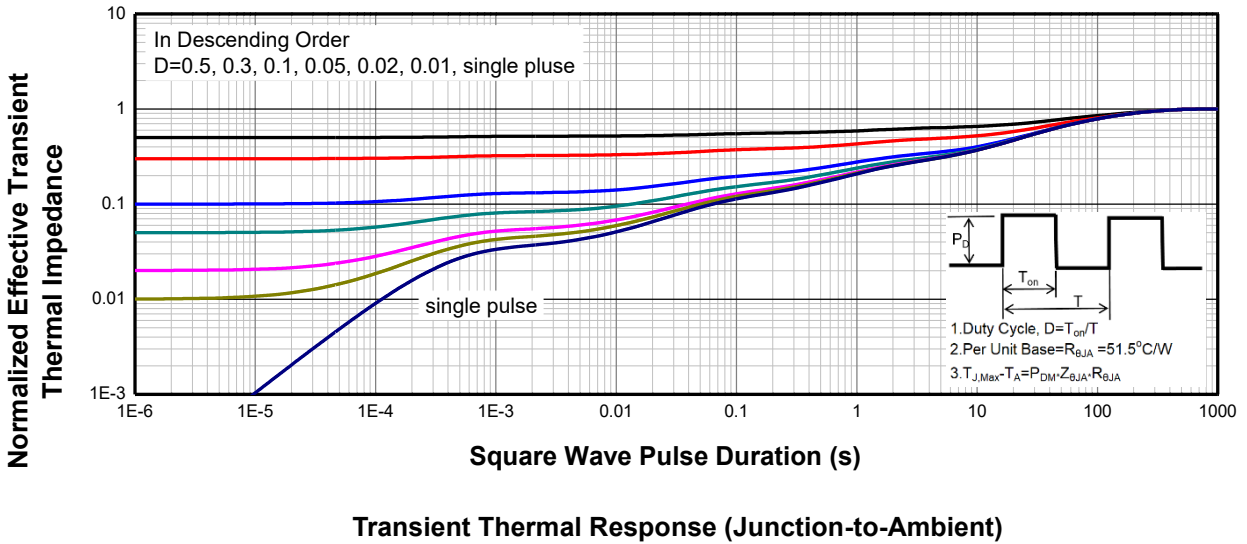
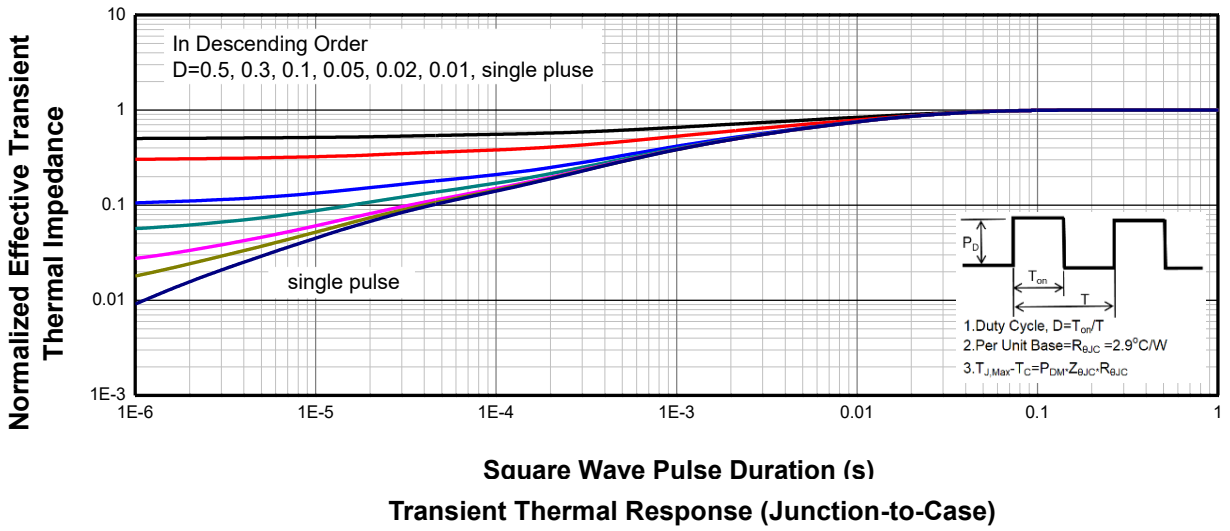
- a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm² area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ $t \leq 10\text{s}$ value and the $T_{J(MAX)}=150^\circ\text{C}$. The value is only for reference, any application depends on the user's specific board design.
- b The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- c Repetitive rating, $\sim 10\mu\text{s}$ pulse width, duty cycle $\sim 1\%$, keep initial $T_J = 25^\circ\text{C}$, the maximum allowed junction temperature of 150°C .
- d The static characteristics are obtained using $\sim 380\mu\text{s}$ pulses, duty cycle $\sim 1\%$.
- e The parameter is not subject to production test – verified by design / characterization.

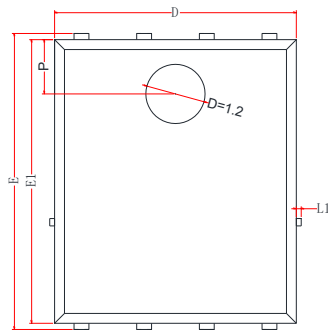
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
Gate-to-source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.2	1.7	2.2	V
Drain-to-source On-resistance ^d	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		2.7	3.4	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		4.1	5.5	
CHARGES, CAPACITANCES AND GATE RESISTANCE^e						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz},$ $V_{DS} = 15\text{ V}$		1669		pF
Output Capacitance	C_{OSS}			705		
Reverse Transfer Capacitance	C_{RSS}			35		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V},$ $I_D = 20\text{ A}$		22.7		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 15\text{ V},$ $I_D = 20\text{ A}$		10.5		
Gate-to-Source Charge	Q_{GS}	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V},$ $I_D = 20\text{ A}$		4.6		
Gate-to-Drain Charge	Q_{GD}	$I_D = 20\text{ A}$		2.0		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.8		Ω
SWITCHING CHARACTERISTICS^e						
Turn-On Delay Time	$t_d(ON)$	$V_{GS} = 10\text{ V},$ $V_{DD} = 15\text{ V},$ $I_D = 20\text{ A}, R_G = 6\Omega$		6.2		ns
Rise Time	t_r			60.5		
Turn-Off Delay Time	$t_d(OFF)$			19.5		
Fall Time	t_f			14.8		
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20\text{ A},$ $dI/dt = 100\text{ A}/\mu\text{s}$		26.1		ns
Body Diode Reverse Recovery Charge	Q_{rr}			16.5		nC
BODY DIODE CHARACTERISTICS						
Forward Voltage ^d	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 1\text{ A}$		0.7	1.2	V
Maximum Continuous Current	I_S				43	A

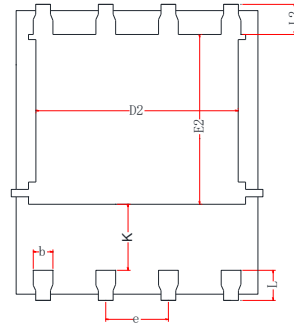
Typical Characteristics (Ta=25°C, unless otherwise noted)

Output Characteristics ^d

Transfer Characteristics ^d

On-Resistance vs. Drain Current ^d

On-Resistance vs. Gate to Source Voltage ^d

On-Resistance vs. Junction Temperature ^d

Threshold Voltage vs. Temperature


Capacitance

Body Diode Forward Voltage^d

Single Pulse Power

Safe Operating Area

Gate Charge Characteristics



PACKAGE OUTLINE DIMENSIONS
PDFN5x6-8L


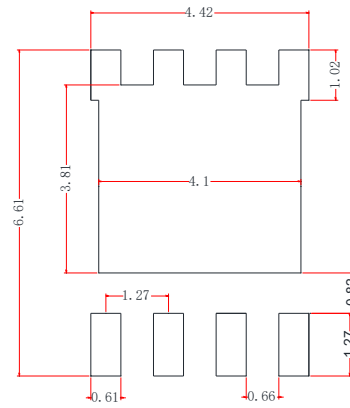
TOP VIEW



BOTTOM VIEW

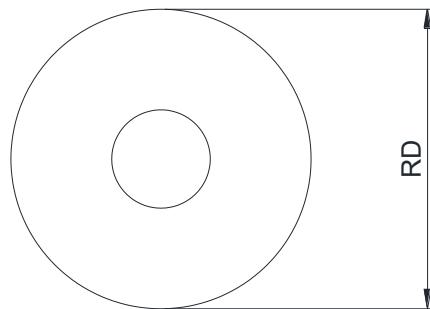
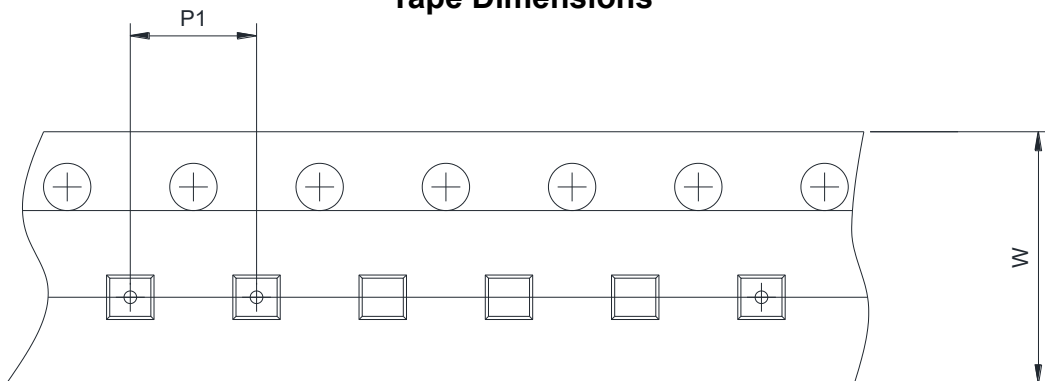
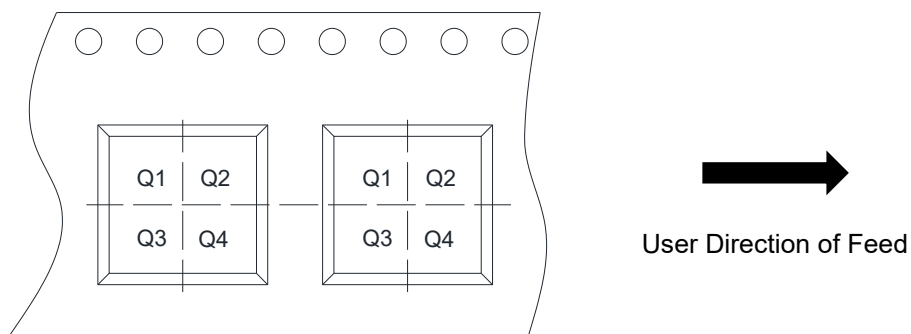


SIDE VIEW



RECOMMENDED LAND PATTERN (Unit:mm)

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	1.00	1.10	1.20
b	0.35	0.40	0.45
c	0.21	0.25	0.34
D	4.80	4.90	5.00
D2	3.82	-	4.11
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.18	-	3.54
e	1.27BSC		
K	1.10	-	-
L	0.51	0.61	0.71
L1	-	-	0.10
L2	0.51	0.61	0.71
P	1.00	1.10	1.20
θ	8°	-	12°

TAPE AND REEL INFORMATION
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input checked="" type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm <input checked="" type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2 <input type="checkbox"/> Q3 <input type="checkbox"/> Q4