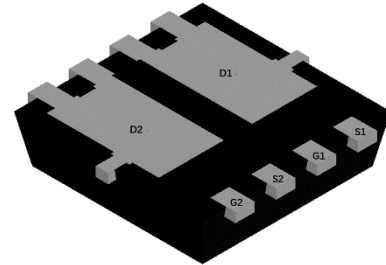
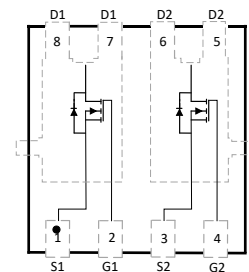
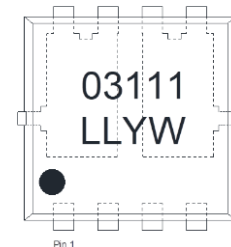


SND0311R5DRA
Dual N-Channel, 30V, 9.8A, Power MOSFET
<http://www.sitcores.com/>

V_{DS} (V)	Max. $R_{DS(on)}$ (m Ω)
30	11.5 @ $V_{GS}=10V$
	15.5 @ $V_{GS}=4.5V$


Description

The SND0311R5DRA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SND0311R5DRA is in compliance with RoHS.

PDFN3333-8L

Pin configuration (Top view)


03111 = Device Code
 LL = Special Code
 Y = Year
 W = Week (A~z)

Marking
Features

- Trench Technology
- Supper high density cell design
- Low ON resistance
- Package PDFN3333-8L
- 100% UIS and Rg Tested
- MSL3

Applications

- DC/DC converters
- Power supply converters circuit
- Power Switching for portable device

Order information

Device	Package	Shipping
SND0311R5DRA-8/TR	PDFN3333-8L	5000/Tape&Reel

Absolute Maximum ratings

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^d	$T_C=25^\circ\text{C}$	9.8	A
	$T_C=100^\circ\text{C}$	9.8	A
Pulsed Drain Current ^c	I_{DM}	90	A
Continuous Drain Current ^d	$T_A=25^\circ\text{C}$	9.8	A
	$T_A=70^\circ\text{C}$	9.8	
Avalanche Energy $L=0.3\text{mH}$	E_{AS}	16.3	mJ
Power Dissipation ^b	$T_C=25^\circ\text{C}$	26	W
	$T_C=100^\circ\text{C}$	11	
Power Dissipation ^a	$T_A=25^\circ\text{C}$	4.1	W
	$T_A=70^\circ\text{C}$	2.6	
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal resistance ratings

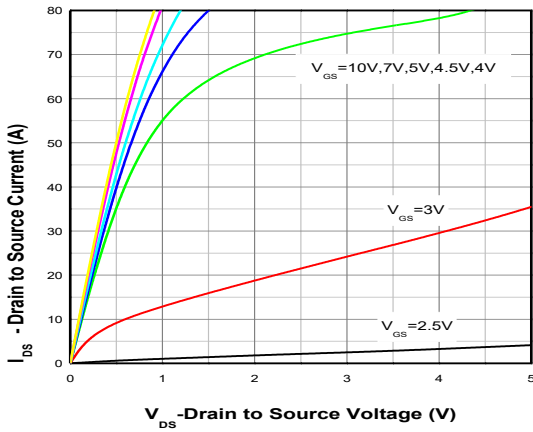
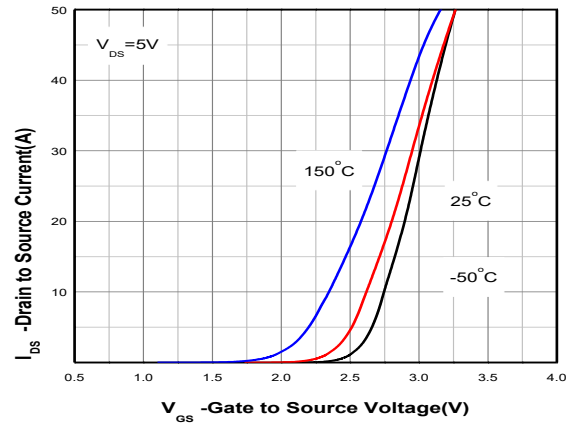
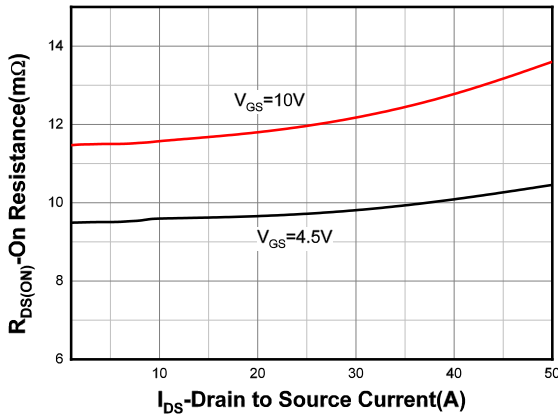
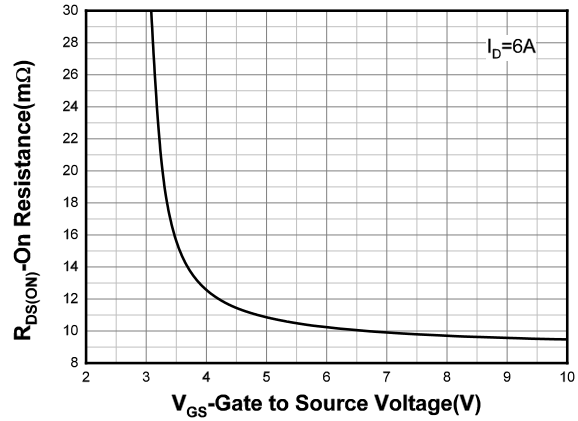
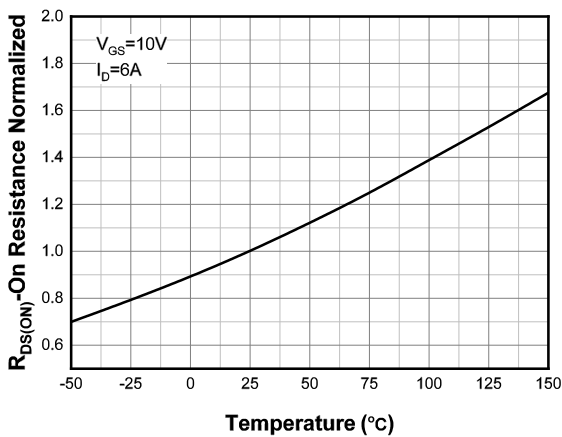
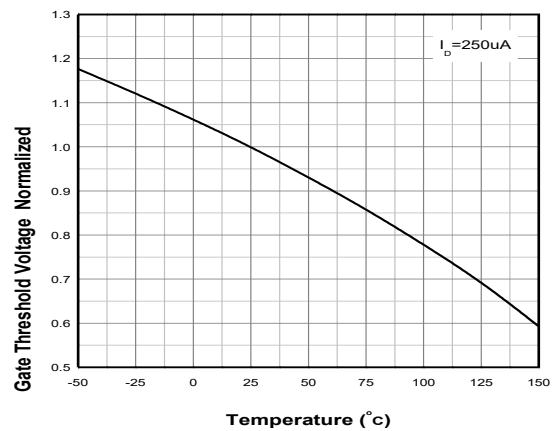
Single Operation					
Parameter	Symbol	Typical	Maximum	Unit	
Junction-to-Ambient Thermal Resistance ^a	$t \leq 10\text{ s}$	24.5	30.5	$^\circ\text{C/W}$	
	Steady State	52.5	65.5		
Junction-to-Case Thermal Resistance	Steady State	3.8	4.8		

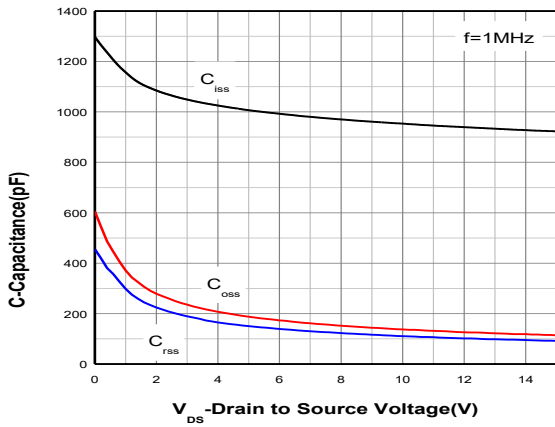
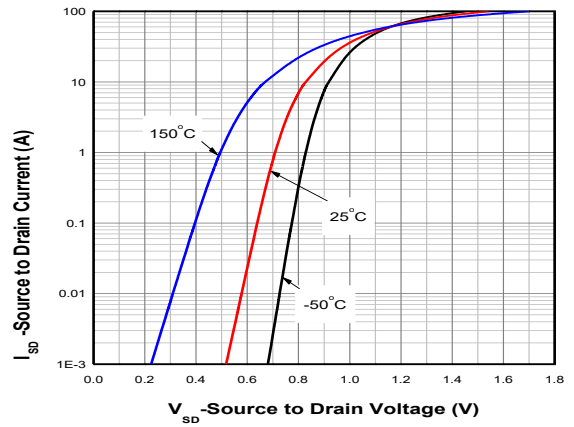
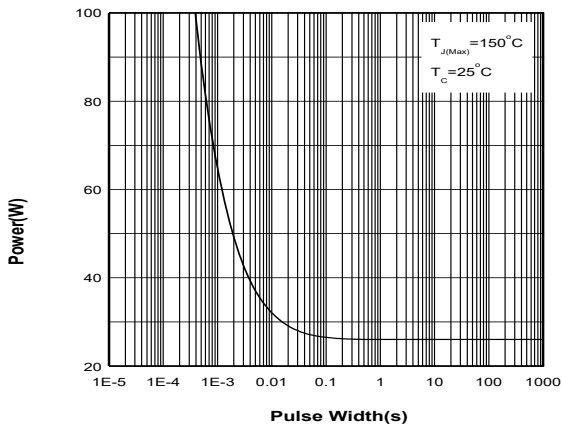
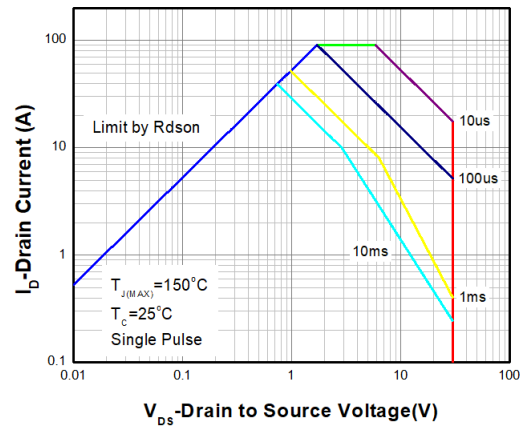
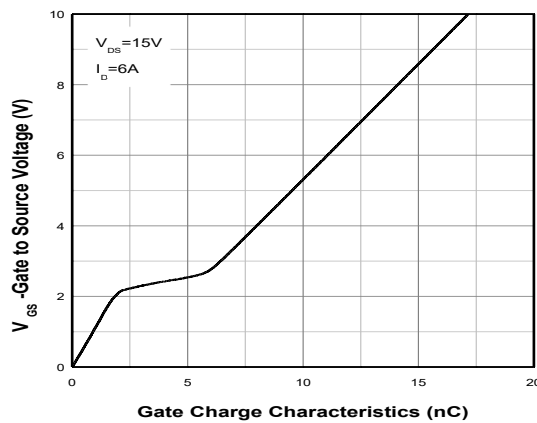
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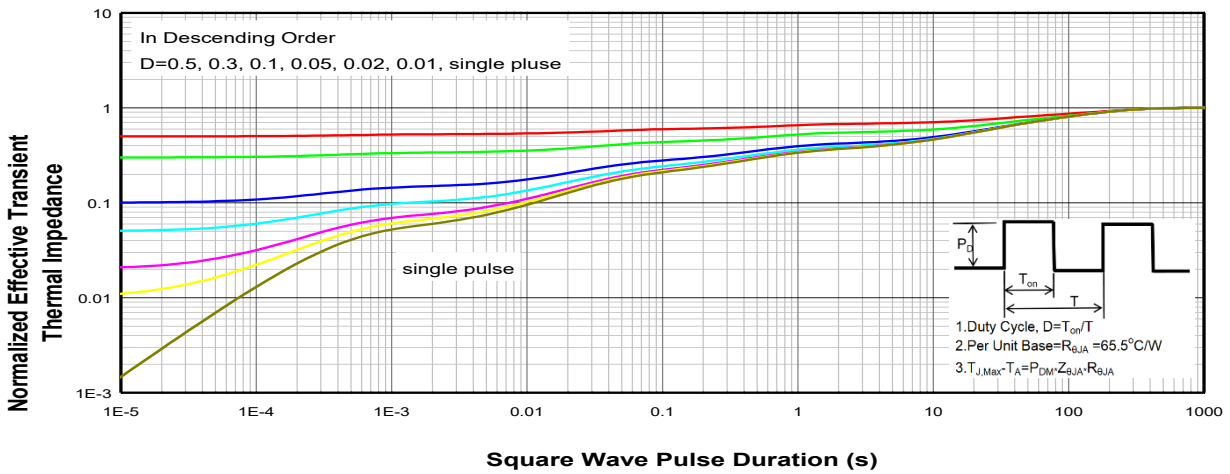
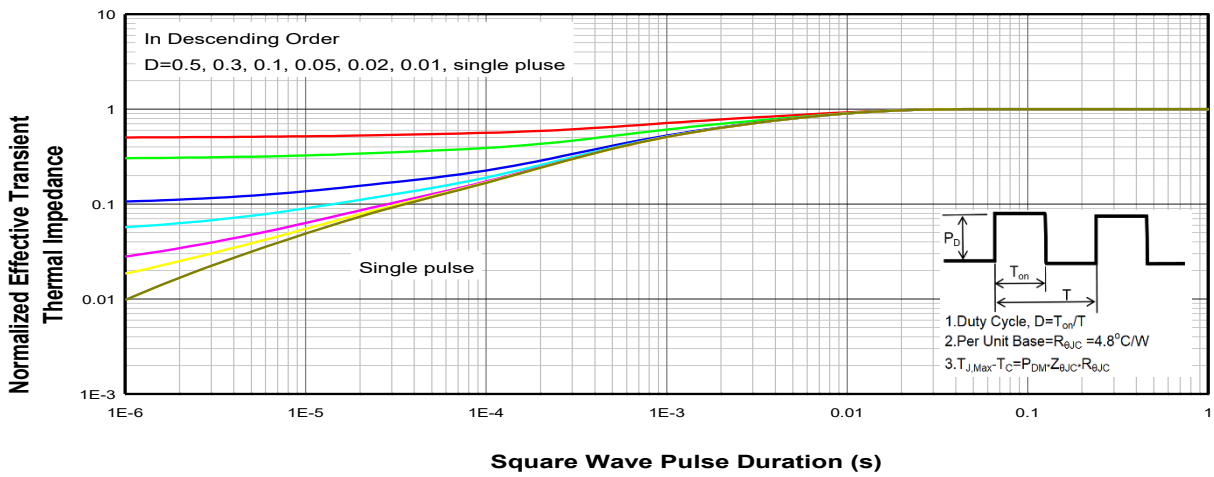
- a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm² area). The power adissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ $t \leq 10\text{s}$ value and the $T_{J(MAX)}=150^\circ\text{C}$. The value is only for reference, any application depends on the user's specific board design.a
- b The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in asetting the upper dissipation limit for cases where additional heat sinking is used.
- c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial $T_J = 25^\circ\text{C}$, the maximum allowed junction temperature of 150°C .
- d The maximum current rating by source bonding technology.
- e The static characteristics are obtained using ~380us pulses, duty cycle ~1%.
- f The parameter is not subject to production test – verified by design / characterization.

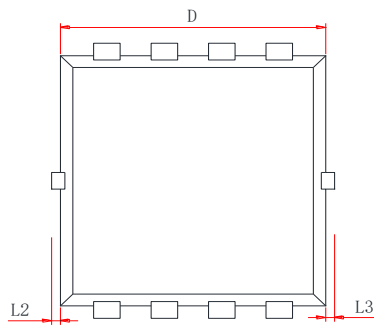
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
Gate-to-source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.1	1.6	2.1	V
Drain-to-source On-resistance ^e	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$		9.5	11.5	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 6\text{ A}$		11.5	15.5	
CHARGES, CAPACITANCES AND GATE RESISTANCE ^f						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		925		pF
Output Capacitance	C_{OSS}			115		
Reverse Transfer Capacitance	C_{RSS}			92		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V}, I_D = 6\text{ A}$		17.2		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 15\text{ V}, I_D = 6\text{ A}$		8.7		
Gate-to-Source Charge	Q_{GS}	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V}, I_D = 6\text{ A}$		2.2		
Gate-to-Drain Charge	Q_{GD}	$I_D = 6\text{ A}$		3.4		
Gate Resistance	R_g	$f = 1\text{ MHz}$		2.1		
SWITCHING CHARACTERISTICS ^f						
Turn-On Delay Time	$t_d(ON)$	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V}, I_D = 6\text{ A}, R_G = 6\Omega$		4.7		ns
Rise Time	t_r			24.4		
Turn-Off Delay Time	$t_d(OFF)$			17.0		
Fall Time	t_f			17.7		
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 6\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		9.1		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$I_F = 6\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		2.8		nC
BODY DIODE CHARACTERISTICS						
Forward Voltage ^e	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 1\text{ A}$		0.7	1.2	V
Maximum Continuous Current ^d	I_S				9.8	A

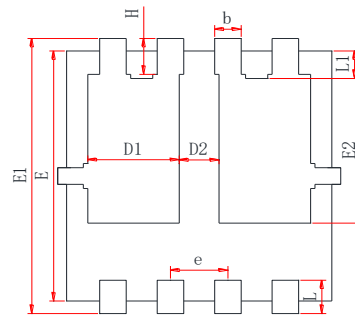
Typical Characteristics (Ta=25°C, unless otherwise noted)

Output Characteristics ^e

Transfer Characteristics ^e

On-Resistance vs. Drain Current ^e

On-Resistance vs. Gate-to-Source Voltage ^e

On-Resistance vs. Junction Temperature ^e

Threshold Voltage vs. Temperature


Capacitance

Body Diode Forward Voltage^e

Single Pulse power

Safe Operating Area

Gate Charge Characteristics

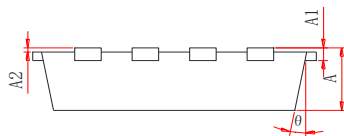


PACKAGE OUTLINE DIMENSIONS
PDFN3333-8L


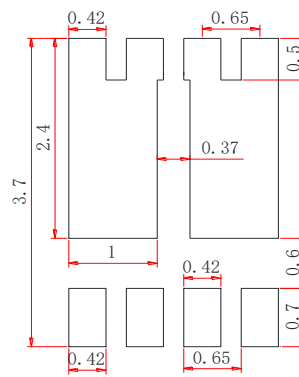
TOP VIEW



BOTTOM VIEW

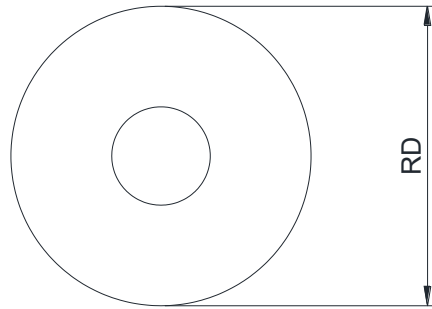
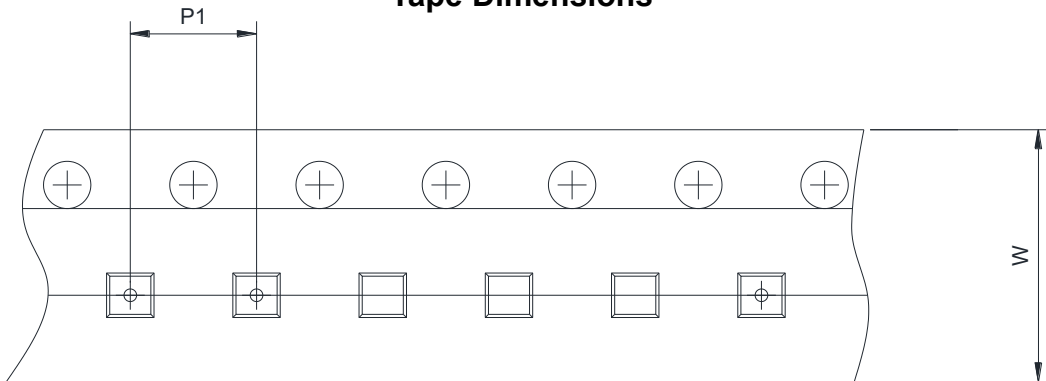
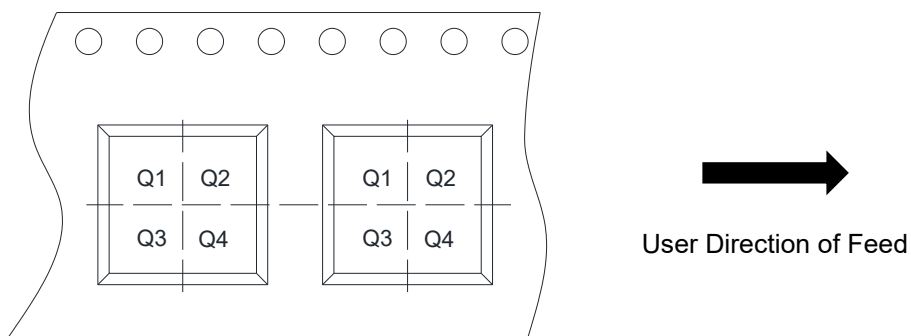


SIDE VIEW



RECOMMENDED LAND PATTERN (unit:mm)

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.65	0.75	0.85
A1	0.152 REF		
A2	0.00	-	0.05
D	2.90	3.00	3.10
D1	0.935	1.035	1.135
D2	0.28	0.38	0.48
E	2.90	3.00	3.10
E1	3.15	3.30	3.45
E2	1.535	1.735	1.935
b	0.20	0.30	0.40
e	0.55	0.65	0.75
L	0.30	0.40	0.50
L1	0.18	0.33	0.48
L2/L3	0.00	-	0.10
H	0.315	0.415	0.515
θ	9°	11°	13°

TAPE AND REEL INFORMATION
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input checked="" type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm <input checked="" type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2 <input type="checkbox"/> Q3 <input type="checkbox"/> Q4