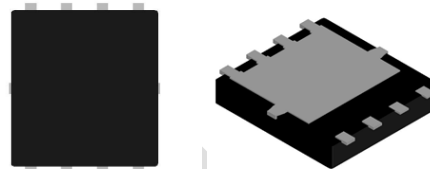


SNM043R15DNAQ

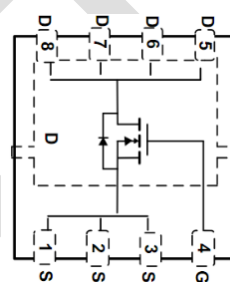
**Single N-Channel, 40V,110A
Power MOSFET**

<http://www.sitcores.com/>

V_{DS} (V)	Max. $R_{DS(on)}$ (m Ω)
40	3.15@ $V_{GS}=10V$



PDFN5X6-8L



Pin Configuration (Top view)



WLSI = Company (Group) Code
 04402 = Device Code
 DN = Special Code
 M = Month
 W = Week

Marking

Description

The SNM043R15DNAQ is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in high performance automotive DC-DC conversion, power switch and charging circuit. Standard Product SNM043R15DNAQ is in compliance with RoHS.

Features

- Automotive applications
- AEC-Q101 Qualified
- Excellent ON resistance
- General footprint package PDFN5X6-8L
- 100% Rg and Avalanche tested
- MSL1

Applications

- Automotive systems
- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
SNM043R15DNA Q-8/TR	PDFN5*6-8L	5000/Tape& Reel

Absolute Maximum ratings ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C=25^{\circ}\text{C}$ 110	A
		$T_C=100^{\circ}\text{C}$ 78	A
Pulsed Drain Current ^c	I_{DM}	267	A
Continuous Drain Current	I_D	$T_A=25^{\circ}\text{C}$ 24	A
		$T_A=100^{\circ}\text{C}$ 17	
Avalanche Energy $L=0.1\text{mH}$	E_{AS}	68.5	mJ
Power Dissipation ^b	P_D	$T_C=25^{\circ}\text{C}$ 67	W
		$T_C=100^{\circ}\text{C}$ 33	
Power Dissipation ^a	P_D	$T_A=25^{\circ}\text{C}$ 3.2	W
		$T_A=100^{\circ}\text{C}$ 1.6	
Operating Junction Temperature	T_J	-55 to 175	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55 to 175	$^{\circ}\text{C}$

Thermal resistance ratings

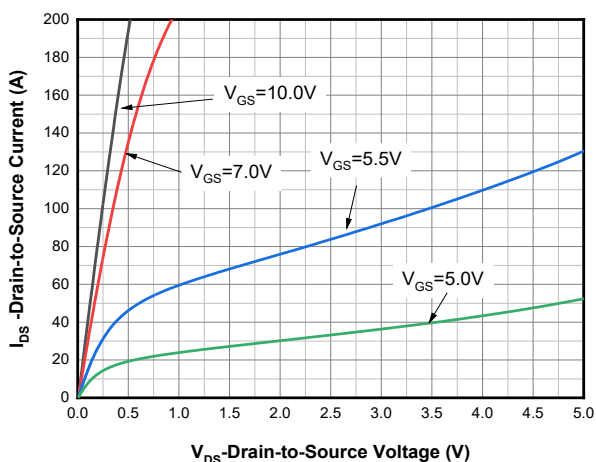
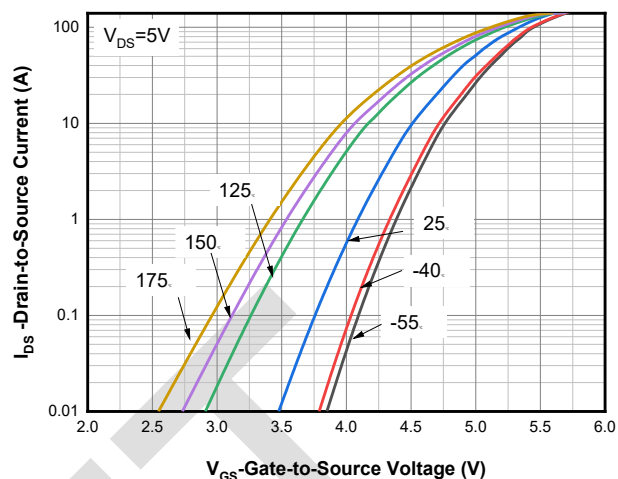
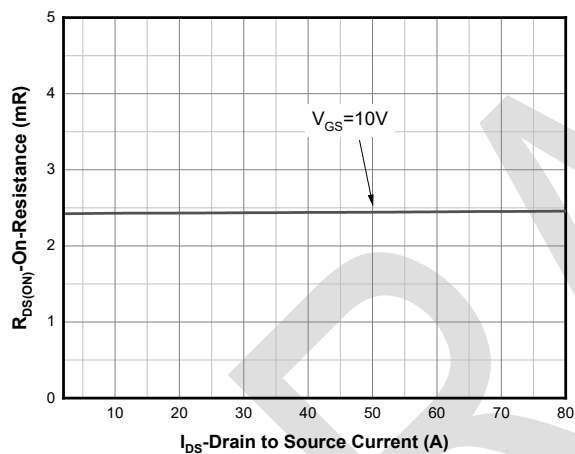
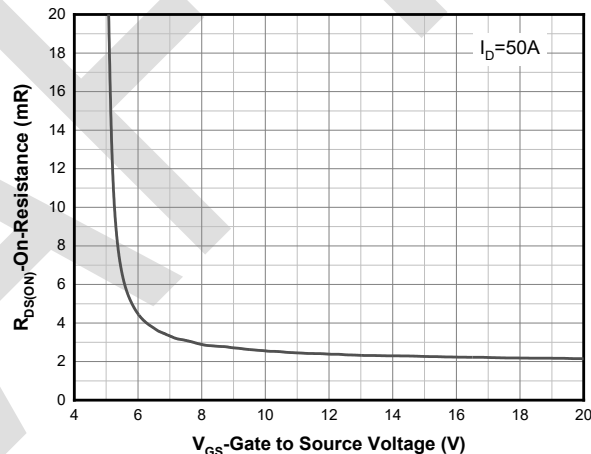
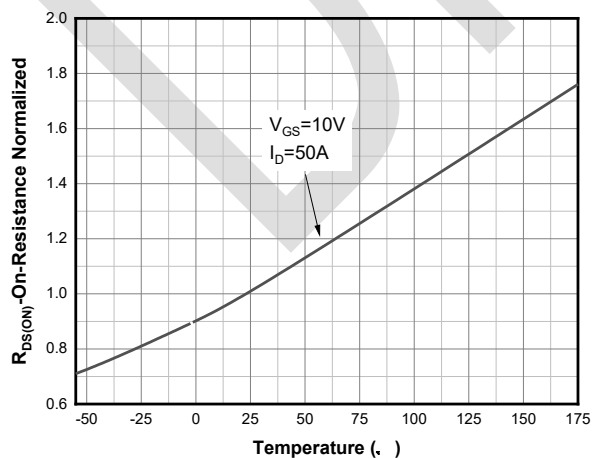
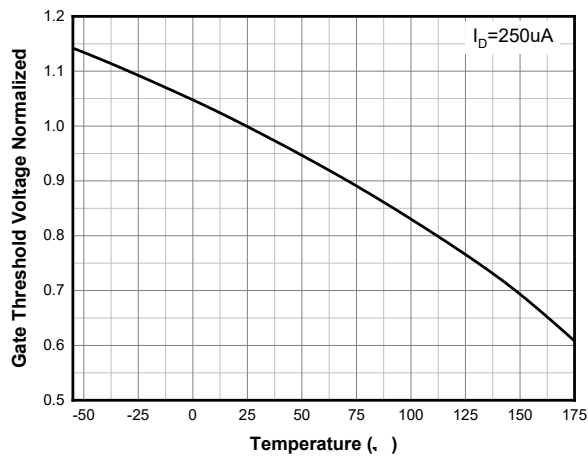
Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ^a	Steady State	$R_{\theta JA}$	38.5	46.2	$^{\circ}\text{C/W}$
Junction-to-Case Thermal Resistance ^b	Steady State	$R_{\theta JC}$	1.6	2.2	

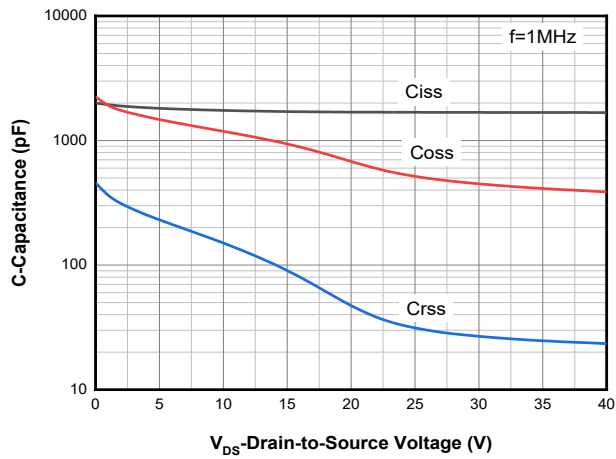
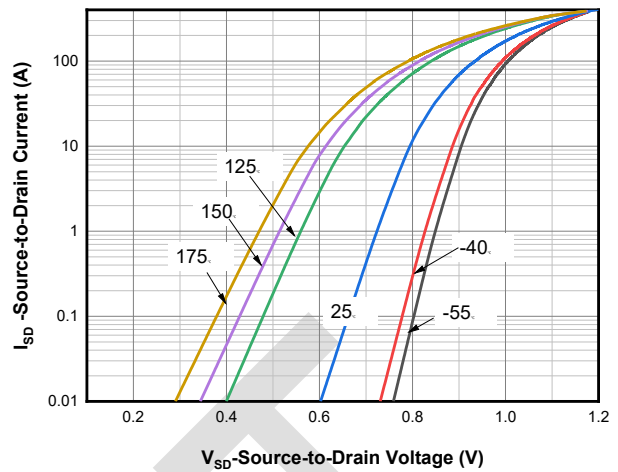
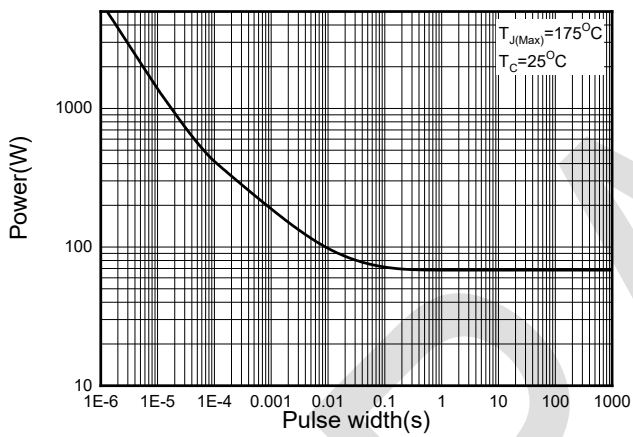
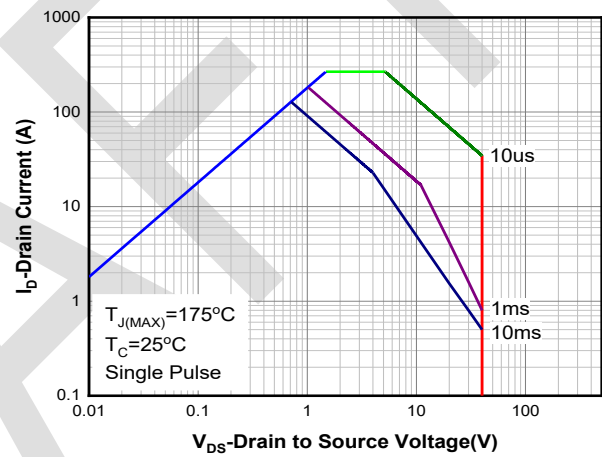
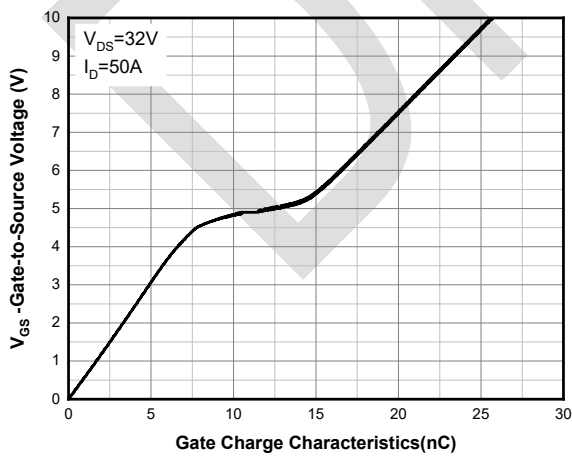
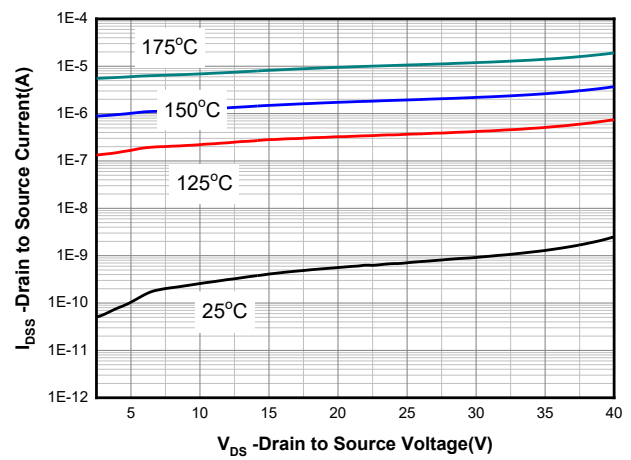
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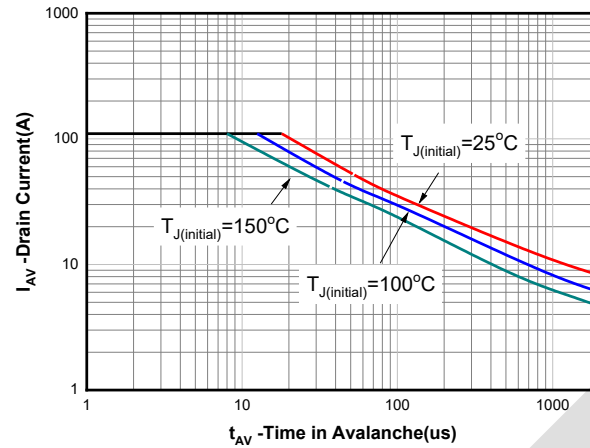
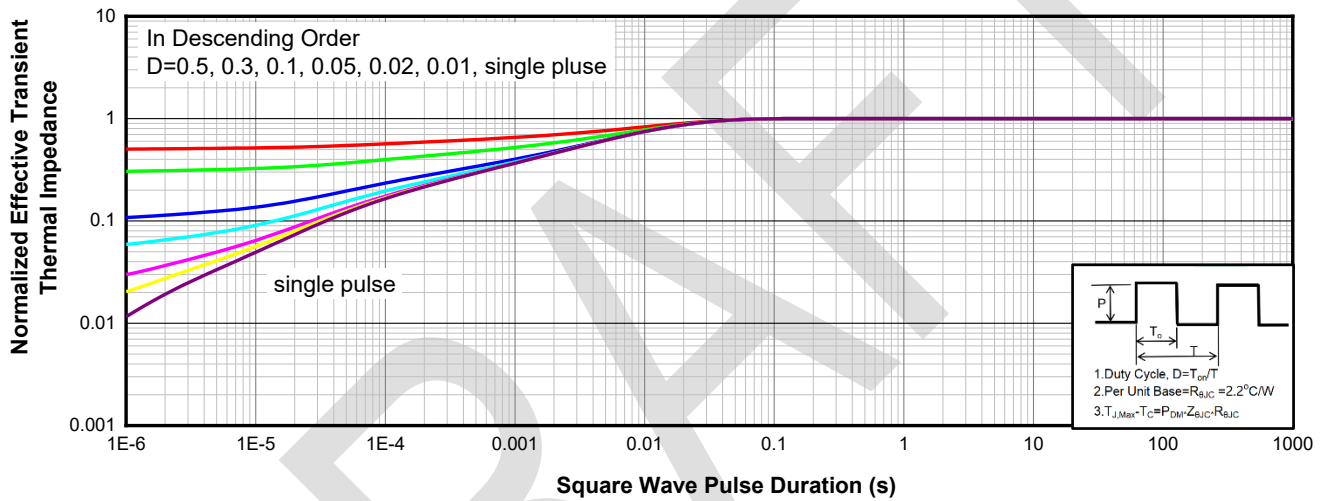
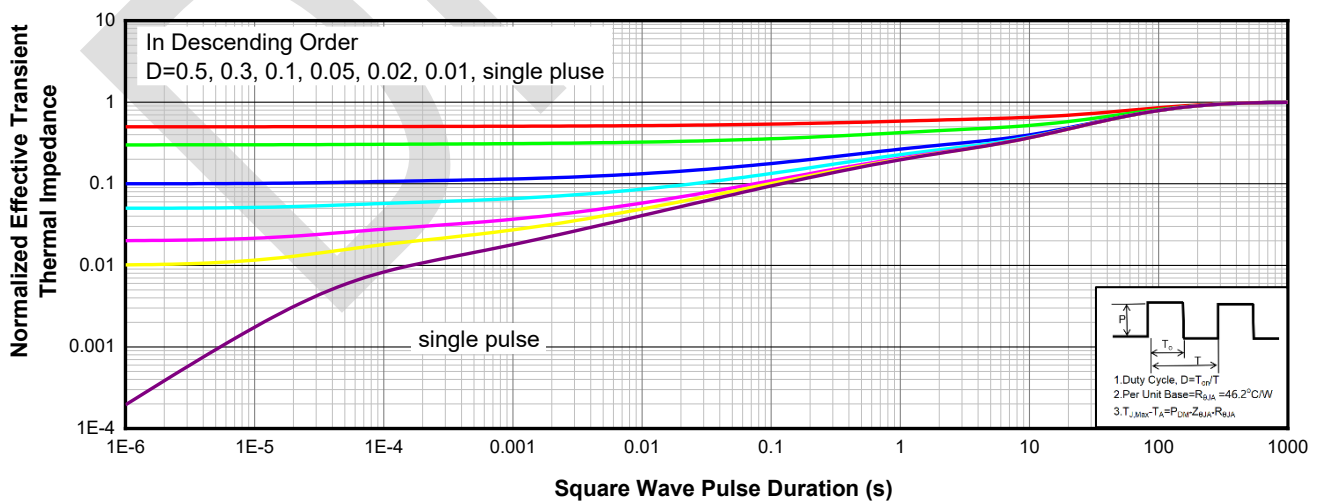
- a FR-4 board (38mm X 38mm X 1.6mm, 70um Copper) partially covered with copper (645mm² area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance value and the $T_{J(MAX)}=175^{\circ}\text{C}$. The value is only for reference, any application depends on the user's specific board design.
- b The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- c Repetitive rating, pulsed, duty cycle ~1%, keep initial $T_J=25^{\circ}\text{C}$, the maximum allowed junction temperature of 175°C .
- d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.
- e The parameter is not subject to production test – verified by design / characterization.

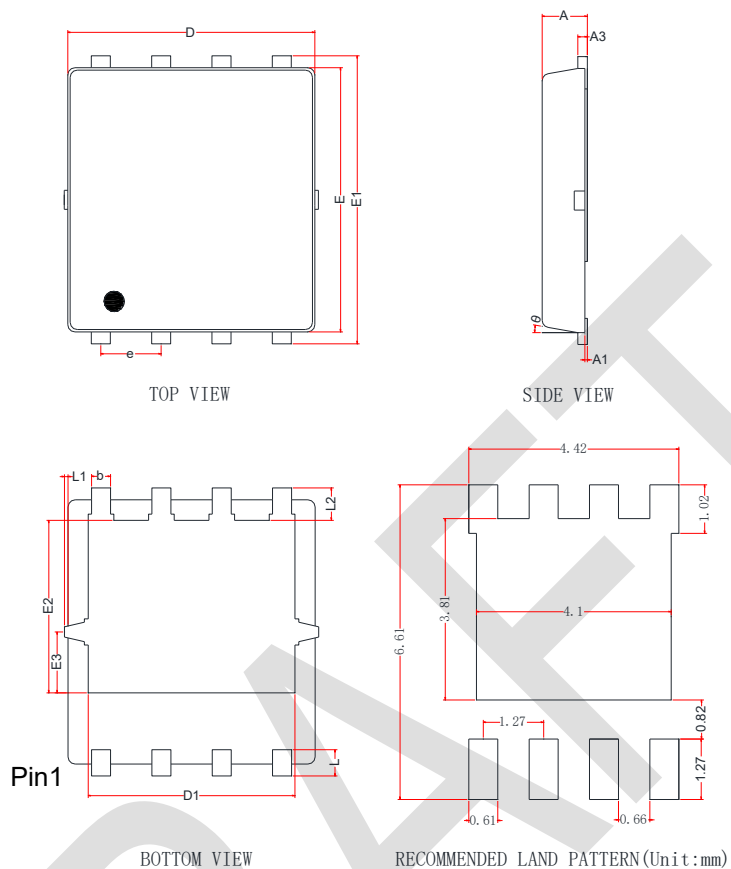
Electronics Characteristics (T_J=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0 V, I _D = 250uA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	BV _{DSS} /T _J			22.1		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =32V, V _{GS} = 0V, T _J =25° C			1	uA
		V _{DS} =32V, V _{GS} = 0V, T _J =125° C			100	uA
Gate-to-source Leakage Current	I _{GSS}	V _{DS} =0 V, V _{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} =V _{DS} , I _D = 250uA	2.4	3.0	3.6	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-6.5		mV/°C
Drain-to-source On-resistance	R _{DS(on)}	V _{GS} =10V, I _D =50A		2.5	3.15	mΩ
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C _{ISS}	V _{GS} =0V, f= 1.0MHz, V _{DS} =25 V		1685		pF
Output Capacitance	C _{OSS}			515		
Reverse Transfer Capacitance	C _{RSS}			31		
Total Gate Charge °	Q _{G(TOT)}	V _{GS} =10V, V _{DS} = 32V, I _D =50 A		27.5		nC
Gate-to-Source Charge °	Q _{GS}			8.7		
Gate-to-Drain Charge °	Q _{GD}			7.0		
Gate Resistance	R _g	f=1MHz		0.8		Ω
SWITCHING CHARACTERISTICS °						
Turn-On Delay Time	td(ON)	V _{GS} =10V, V _{DS} = 32V, I _D =50A, R _G =5Ω		10.6		ns
Rise Time	tr			35.6		
Turn-Off Delay Time	td(OFF)			21.2		
Fall Time	tf			15.0		
Body Diode Reverse Recovery Time	trr	I _F =50A, dI/dt=100A/μs		33.8		ns
Body Diode Reverse Recovery Charge	Q _{rr}	I _F =50A, dI/dt=100A/μs		20.9		nC
BODY DIODE CHARACTERISTICS						
Forward Voltage ^d	V _{SD}	V _{GS} =0 V, I _S =50A	0.5	0.8	1.2	V

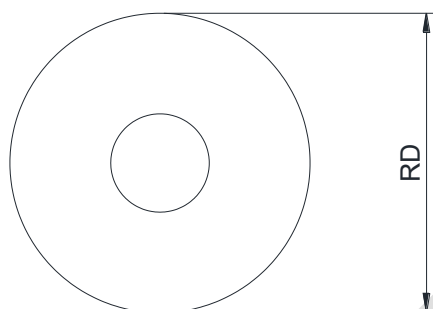
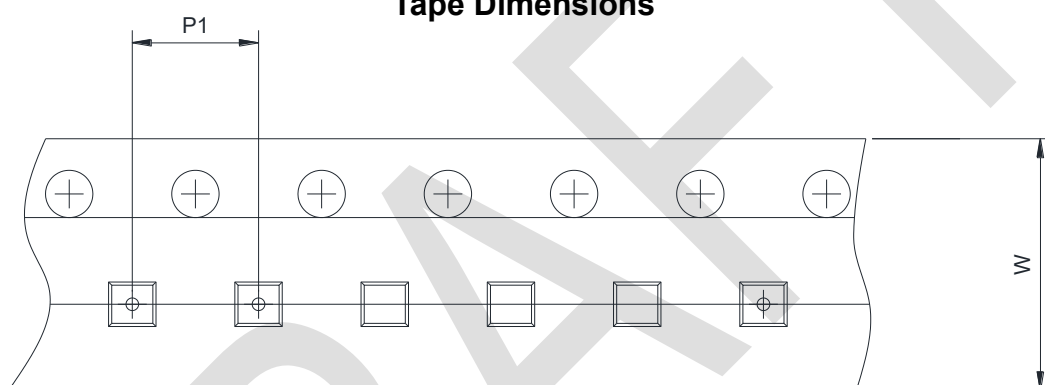
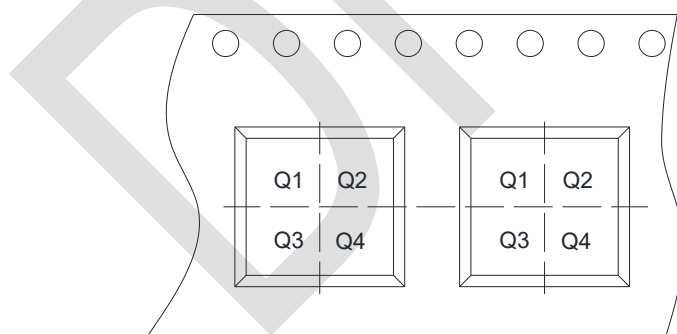
Typical Characteristics (Ta=25°C, unless otherwise noted)

Output Characteristics ^d

Transfer Characteristics ^d

On-Resistance vs. Drain Current ^d

Transfer Characteristics ^d

On-Resistance vs. Junction Temperature ^d

Threshold Voltage vs. Temperature


Capacitance

Body Diode Forward Voltage ^d

Single Pulse power

Safe Operating Area

Gate Charge Characteristics

Drain Current vs. Drain Voltage


Avalanche characteristics

Transient Thermal Response (Junction-to-Case)

Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS
PDFN5X6-8L


Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.85	0.95	1.00
A1	0.00	---	0.05
A3	---	0.2 Ref	---
b	0.30	0.40	0.50
D	5.10	5.20	5.30
E	5.45	5.55	5.65
e	1.27 BSC		
D1	4.25	4.35	4.45
E1	5.95	6.05	6.15
E2	3.525	3.625	3.725
E3	1.175	1.275	1.375
L	0.45	0.55	0.65
L1	0	---	0.15
L2	0.68 Ref		
θ	0 °	---	10 °

TAPE AND REEL INFORMATION
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


➔
User Direction of Feed

RD	Reel Dimension	☐ 7inch	☒ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☒ 12mm		
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☒ 8mm	
Pin1	Pin1 Quadrant	☒ Q1	☐ Q2	☐ Q3	☐ Q4