FEATURES

- Compliant with ISO 11898-2:2016 standard
- AEC-Q100 qualified
- Support 5Mbit/s CAN FD rate
- Autonomous bus biasing function
- Very low power sleep/standby mode with bus remote wake-up capability
- Integrated 5V output voltage regulator V1 by BAT input, output voltage accuracy ±2%, current limiting >150mA, undervoltage reset with selectable detection thresholds of 60%, 70%, 80% or 90% of output voltage
- Overtemperature warning and shutdown
- Power-on and power-off detection function on BAT pin
- Transmit data (TXD) dominant time-out function
- CAN bus terminal current limit protected
- Mode control via the Serial Peripheral Interface (SPI)
- Integrated with multiple fail-safe and reset functions, corresponding register bit information can be queried via SPI
- Built-in non-volatile memory for user-customizable initialization functions
- Integrated watchdog with Window, Timeout and Autonomous modes
- Integrated local wake-up via WAKE pin
- Integrated high voltage INH pin
- CAN bus pins short-circuit proof to ±58V
- Virtual junction temperature: -40℃ to 150℃
- High ElectroMagnetic Immunity (EMI)
- Available in leadless DFN4.5*3-14 package, and the package with improved Automated Optical Inspection (AOI)capability

DESCRIPTION

The SIT1167Q is a mini high-speed CAN System Basis Chip (SBC) containing an ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant HS-CAN transceiver and an integrated 5V/100mA supply for a microcontroller. It also features a watchdog and a Serial Peripheral Interface (SPI). The SIT1167Q can be operated in very-low-current Standby and Sleep modes with bus and local wake-up capability and supports ISO 11898-2:2016 compliant autonomous CAN biasing.

The system controller contains a state machine that supports seven operating modes: Normal, Standby, Sleep, Reset, Forced Normal, Overtemp and Off.

PINNING INFORMATION

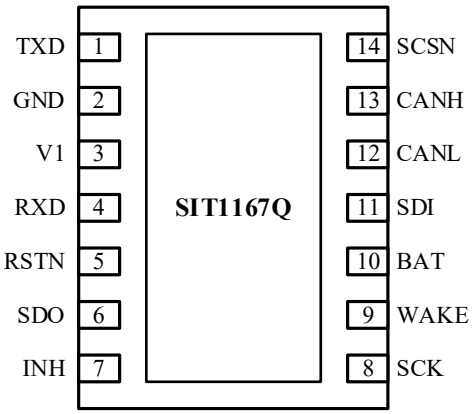


Figure 1 Pin configuration diagram

PIN DESCRIPTION

PIN	Symbol	Description
1	TXD	transmit data input
2	GND	ground
3	V1	5 V microcontroller supply voltage
4	RXD	receive data output; reads out data from the bus lines
5	RSTN	reset input/output
6	SDO	SPI data output
7	INH	high-voltage output for switching external regulators
8	SCK	SPI clock input
9	WAKE	local wake-up input
10	BAT	battery supply voltage
11	SDI	SPI data input
12	CANL	LOW-level CAN bus line
13	CANH	HIGH-level CAN bus line
14	SCSN	SPI chip select input

Note: The metal pad on the back of the DFN4.5*3-14 package is recommended to be grounded.

LIMITING VALUES

Symbol	Parameter	Conditions	SPEC	Unit
V_X	Voltage on pin x	Pin V1	-0.3 ~ +6	V
		Pins TXD, RXD, SDI, SDO, SCK, SCSN, RSTN	-0.3 ~ V_{V1}+0.3	V
		Pins INH, WAKE	-18 ~ +40	V
		Pin BAT	-0.3 ~ +40	V
		Pins CANH, CANL	-58 ~ +58	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-40 ~ +40	V
V_{ESD}	ElectroStatic Discharge	IEC 61000-4:2: pins CANH and CANL	-8~+8	kV
		HBM, All pins	-4~+4	kV
		HBM, pins CANH and CANL	-8~+8	kV
		CDM, all pins	-2~2	kV
T_j	Virtual junction temperature		-40 ~ 150	ºC
		when programming the MTPNV cells	0 ~ +125	ºC
T_{stg}	Storage temperature	T_{stg}	-55 ~ +150	ºC

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DFN4.5*3-14	36	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	DFN4.5*3-14	32	°C/W

BLOCK DIAGRAM

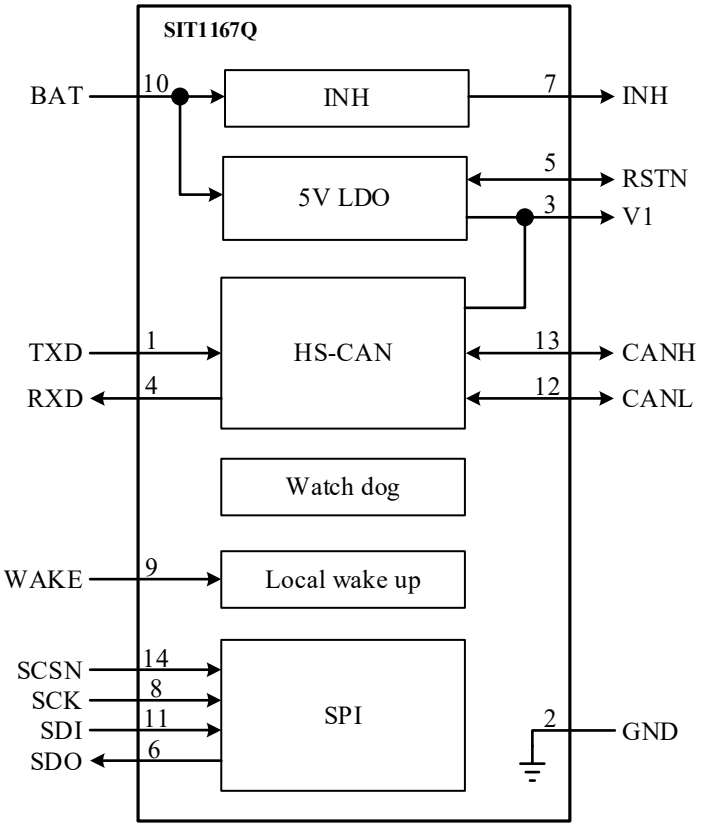


Figure 2 SIT1167Q Block diagram

FUNCTIONAL DESCRIPTION

1 System mode

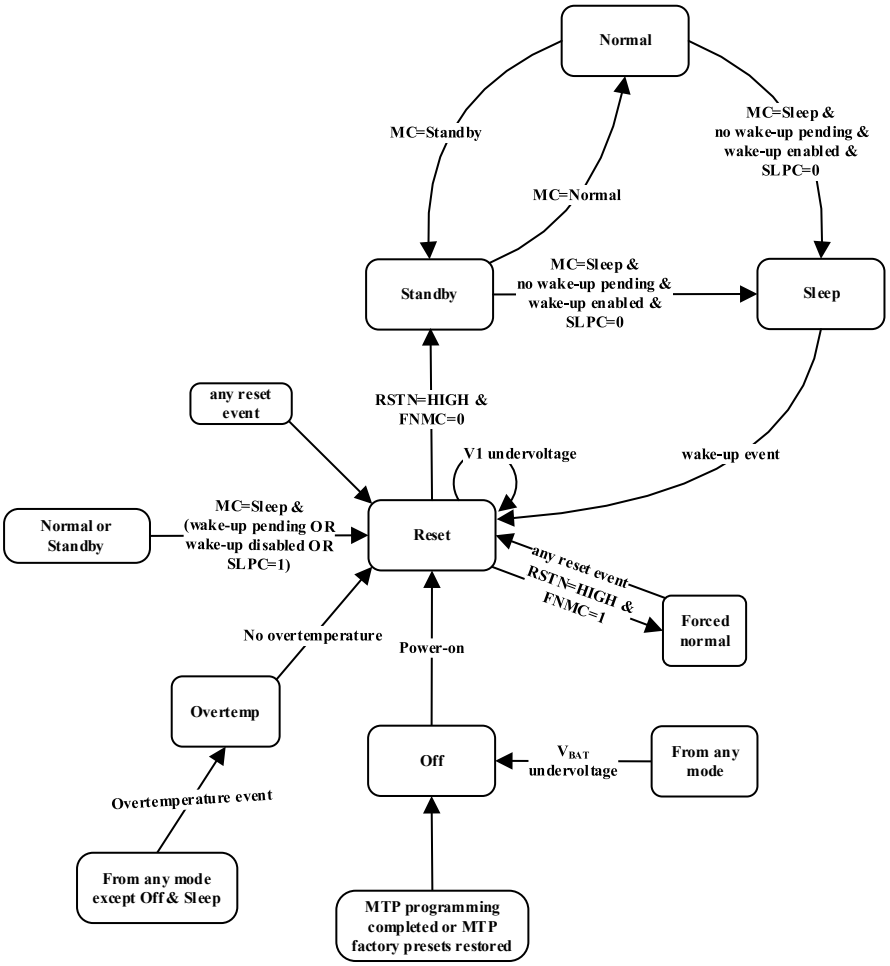


Figure 3 SIT1167Q system controller state diagram

1.1 Off mode

The SIT1167Q switches to Off mode when the initial power on, from any mode when $V_{BAT} < V_{th(det)poff}$, MTP programming completed or MTP factory presets restored. Only power-on detection is enabled; all other modules are inactive. The SIT1167Q starts to boot up when the battery voltage rises above the power-on detection threshold $V_{th(det)pon}$ and switches to Reset mode after $t_{startup}$. In Off mode, the CAN pins disengage from the bus (zero load; high-ohmic).

1.2 Reset mode

Reset mode is the reset state of the SBC. In Reset mode, Pin RSTN is pulled down for a defined time to allow

the microcontroller to start up in a controlled manner.

The SPI is inactive; the watchdog is disabled; V1 and overtemperature detection are active. The transceiver is unable to transmit or receive data in Reset mode. The behavior of INH is determined by the settings of bits VEXTC and VEXTSUC.

The SIT1167Q switches to Reset mode from any mode in response to a reset event (see **Table 3**):

- power-on
- CAN wake-up in Sleep mode
- wake-up via WAKE pin in Sleep mode
- watchdog overflow in Sleep mode (Timeout mode)
- diagnostic wake-up in Sleep mode
- watchdog triggered too early (Window mode)
- watchdog overflow (Window mode or Timeout mode with WDF = 1)
- illegal watchdog mode control access
- RSTN pulled down externally
- exited Overtemp mode
- V1 undervoltage
- illegal Sleep mode command received

If a V1 undervoltage event forced the transition to Reset mode, the SIT1167Q will remain in Reset mode until the voltage on pin V1 has recovered.

The SIT1167Q exits Reset mode:

- switches to Standby mode if pin RSTN is released HIGH
- switches to Forced Normal mode if bit FNMC = 1
- if the SBC is forced into Off or Overtemp mode

1.3 Overtemp mode

Overtemp mode is provided to prevent the SIT1167Q being damaged by excessive temperatures. The SIT1167Q switches to Overtemp mode from any mode except Off mode or Sleep mode when the global chip temperature rises above the overtemperature protection activation threshold $T_{th(act)otp}$.

To help prevent the loss of data due to overheating, the SIT1167Q issues a warning when the IC temperature rises above the overtemperature warning threshold $T_{th(warn)otp.}$ When this happens, status bit OTWS is set and an overtemperature warning event is captured (OTW = 1), if enabled (OTWE = 1).

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. No wake-up event will be detected, but a pending wake-up will still be signaled by a LOW level on pin RXD, which will persist after the overtemperature event has been cleared. When the SBC enters Overtemp mode, V1 is off, pin RSTN is driven LOW and pin INH remains unchanged.

The SIT1167Q exits Overtemp mode:

- switches to Reset mode if the chip temperature falls below the overtemperature protection release threshold $T_{th(rel)otp}$
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

1.4 Force Normal mode

Forced Normal mode is SBC testing mode and is useful for initial prototyping and failure detection, as well as first flashing of the microcontroller. In Forced Normal mode, the watchdog is disabled. The low-drop voltage regulator V1 is active, INH is enabled and the CAN transceiver is active.

Bit FNMC is factory preset to 1, the SIT1167Q initially boots up in Forced Normal mode.This allows a newly installed device to be run in Normal mode without a watchdog. So the microcontroller can be flashed via the CAN bus in the knowledge that a watchdog timer overflow will not trigger a system reset. The non-volatile memory is store bit FNMC (address 74h). So once bit FNMC is programmed to 0, the SBC will no longer boot up in Forced Normal mode, allowing the watchdog to be enabled (see **Table 8**).

Even in Forced Normal mode, a reset event will trigger a transition to Reset mode with normal Reset mode behavior except that the transmitter remains active if there is no V1 undervoltage. However, the SIT1167Q will return to Forced Normal mode instead of switching to Standby mode when it exits Reset mode.

The SIT1167Q exits Force Normal mode:

- switches to Overtemp mode if the chip temperature rises above the overtemperature protection activation threshold $T_{th(act)otp}$
- switches to Reset mode if RSTN pulled down externally, exited Overtemp mode or V1 undervoltage
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

In Forced Normal mode, only the Main status register, the Watchdog status register, the Identification register and registers stored in non-volatile memory can be read. The non-volatile memory area is fully accessible for writing as long as the SIT1167Q is in the factory preset state.

1.5 Standby mode

Standby mode is the first-level power-saving mode of the SIT1167Q, offering reduced current consumption. In Standby mode, the transceiver is unable to transmit or receive data, the V1 is still active and the SPI remains enabled; the watchdog is active in Timeout mode if enabled. The behavior of INH is determined by the SPI setting.

If remote CAN wake-up is enabled (CWE = 1), the receiver monitors bus activity for a wake-up request. Pin RXD is forced LOW when any enabled wake-up event is detected. This can be either a regular wake-up or a diagnostic wake-up such as an overtemperature event. The bus pins are biased to GND (via $R_{i(cm)}$) when the bus is inactive for $t > t_{to(silence)}$ and at approximately 2.5 V when there is activity on the bus (autonomous biasing).

The SIT1167Q switches to Standby mode via Reset mode:

- from Off mode if the battery voltage rises above the power-on detection threshold ($V_{th(det)pon}$)
- from Overtemp mode if the chip temperature falls below the overtemperature protection release threshold $T_{th(rel)otp}$
- from Sleep mode on the occurrence of a regular or diagnostic wake-up event Standby mode can also be selected from Normal mode via an SPI command (MC = 100).

1.6 Normal mode

Normal mode is the active operating mode. In normal mode, all the hardware on the device is available and can be activated (see **Table 1**). Voltage regulator V1 is enabled to supply the microcontroller.

Depending on the SPI register settings, the watchdog may be running in Window or Timeout mode and the INH output may be active. The CAN interface can be configured to be active and thus to support normal CAN communication.

Normal mode can be selected from Standby mode via an SPI command (MC = 111).

1.7 Sleep mode

Sleep mode is the second-level power-saving mode of the SIT1167Q. The difference between Sleep and Standby modes is that V1 is off in Sleep mode and temperature protection is inactive. Any enabled regular wake-up via CAN or WAKE or any diagnostic wake-up event will cause the SIT1167Q to wake up from Sleep mode.

The behavior of INH is determined by the SPI settings. The SPI is disabled. Autonomous bus biasing is active. In sleep mode, watchdog behavior determined by WMC setting (address 00h) and SDMC (see **Table 7**).

The SIT1167Q will switch to Sleep mode when Sleep mode can be selected from Normal or Standby mode via an SPI command (MC = 001), provided there are no pending wake-up events and at least one regular wake-up source is enabled. Any attempt to enter Sleep mode while one of these conditions has not been met will cause the SIT1167Q to switch to Reset mode and set the reset source status bits (RSS = 10100, 'illegal Sleep mode command received'; see **Table 3**).

Since V1 is off in Sleep mode, the only way the SBC can exit Sleep mode is via a wake-up event.

Sleep mode can be permanently disabled in applications where, for safety reasons, the supply voltage to the host controller must never be cut off. Sleep mode is permanently disabled by setting the Sleep control bit SLPC

set in the SBC configuration register (see **Table 8**). This register is located in the non-volatile memory area of the device. When SLPC set, a Sleep mode SPI command (MC = 001) triggers an SPI failure event instead of a transition to Sleep mode.

Table 1 Hardware characterization by functional block

Block	Operating mode						
	Off	**Forced Normal**	**Standby**	**Normal**	**Sleep**	**Reset**	**Overtemp**
V1	Off(1)	On	On	On	Off	On	Off
INH	Off	On	Determined by bits VEXTC and VEXTSUC	Determined by bits VEXTC and VEXTSUC	Determined by bits VEXTC and VEXTSUC	Determined by bits VEXTC and VEXTSUC	unchanged
RSTN	LOW	HIGH	HIGH	HIGH	LOW	LOW	LOW
SPI	Disabled	Active(2)	Active	Active	Disabled	Disabled	Disabled
Watchdog	Off	Off	Determined by bit WMC(3)	Determined by bit WMC	Determined by bit WMC(3)	Off	Off
CAN	Off	Active	Offline	Active/Offline/ Listen-only (determined by bits CMC)	Offline	Offline	Off
RXD	V1 level	CAN bit stream	V1 level/LOW if wake-up detected	CAN bit stream if CMC=01/10/11; otherwise, same as Standby/Sleep	V1 level/LOW if wake-up detected	V1 level/LOW if wake-up detected	V1 level/LOW if wake-up detected

(1) When the SBC switches from Reset, Standby or Normal mode to Off mode in the 5 V variants, V1 behaves as a current source during power down while VBAT is falling from Vth(det)pof down to 2 V (RAM retention feature; see Section 10.1).

(2) Limited register access: Main status register, Watchdog status register, Identification register and non-volatile memory only.

(3) Window mode is only active in Normal mode.

2 System mode control

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 01h.

Table 2 Mode control register (address 01h)

Bit	Symbol	Access	Value	Description
7:3	Reserved	R	-	
2:0	MC	R/W		Mode control:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

3 System mode state

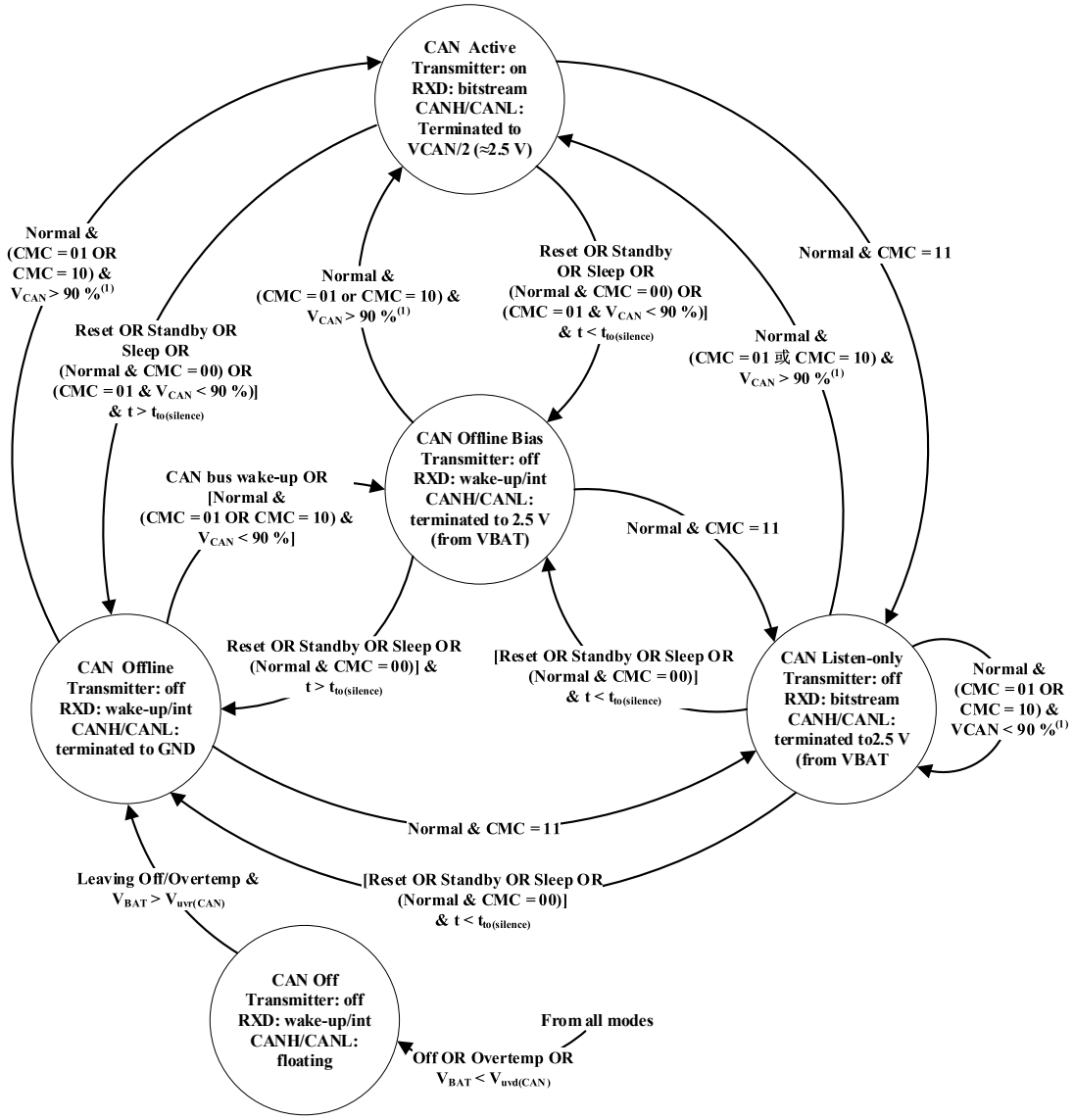
In Main status register, the OTWS can be accessed to monitor the status of the overtemperature warning flag. The NMS to determine whether the SIT1167Q has entered Normal mode after initial power-up. The RSS also indicates the source of the most recent reset event.

Table 3 Main status register (address 03h)

Bit	Symbol	Access	Value	Description
7	Reserved	R	-	
6	OTWS	R		Overtemperature warning status:
			0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	SIT1167Q has entered Normal mode (after power-up)
			1	SIT1167Q has powered up but has not yet switched to Normal mode
4:0	RSS	R		Reset source status:
			00000	Exited Off mode (power-on)
			00001	CAN wake-up in Sleep mode
			00100	Wake-up via WAKE pin in Sleep mode
			01100	Watchdog overflow in Sleep mode (Timeout mode)
			01101	Diagnostic wake-up in Sleep mode
			01110	Watchdog triggered too early (Window mode)
			01111	Watchdog overflow (Window mode or Timeout mode with WDF=1)
			10000	Illegal watchdog mode control access
			10001	RSTN pulled down externally
			10010	Exited Overtemp mode
			10011	V1 undervoltage
			10100	Illegal Sleep mode command received

4 CAN operating modes

The integrated CAN transceiver supports five operating modes: Off, Offline and Offline Bias, Listen-only, Active (see **Figure 4**). The CAN transceiver operating mode depends on the SIT1167Q operating mode and on the setting of bits CMC in the CAN control register.



(1) To prevent the bus lines being driven to a permanent dominant state, the transceiver will not switch to CAN Active mode or CAN Listen-only mode if pin TXD is held LOW (e.g. by a short-circuit to GND)

Figure 4 CAN transceiver state machine (with FNMC = 0)

4.1 CAN Off mode

If one of the following conditions is met, the CAN transceiver will switch to CAN Off:

- V_{BAT} is lower than undervoltage detection threshold, $V_{uvd(CAN)}$
- CAN mode is Off or Overtemp

If V_{BAT} rises above the undervoltage recovery threshold ($V_{uvr(CAN)}$), the CAN transceiver will switch to CAN Offline mode. The battery supply to the SBC is lost so that the CAN transceiver prevents reverse currents flowing from the bus in CAN Off mode.

4.2 CAN Offline and Offline Bias mode

If the transceiver captures the CAN bus for a wake-up event, CAN wake-up detection will be enabled (CWE = 1) in CAN Offline mode. CANH and CANL are bias to GND.

The CAN Offline Bias mode is the same as CAN Offline mode, but the CAN bus bias is 2.5V.

When the transceiver is in CAN Offline mode and activity is detected on the CAN bus, this is automatically activated. The transceiver will return to CAN Offline mode when the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

There are four ways to CAN Offline Bias mode or CAN Offline mode:

- If one of the following conditions is met, the CAN transceiver switches to CAN Offline/Offline Bias mode from CAN Active mode:

  CMC = 01 and V_{CAN} drops lower than the 90 % undervoltage threshold or

  CMC = 10 and V1 drops lower than the V1 reset threshold.

- If one of the following conditions is met, the CAN transceiver will switch from CAN Offline mode to CAN Offline Bias mode:

  a standard wake-up pattern is detected on the CAN bus or

  CAN mode is Normal, CMC = 01 or 10 and V_{CAN} < 90 %

- If one of the following conditions is met, the CAN transceiver switches to CAN Offline mode:

  CAN mode is from Off or Overtemp mode to Reset mode or

  from CAN Offline Bias mode if no activity is detected on the bus (no CAN edges) for $t > t_{to(silence)}$

- If one of the following conditions is met, the CAN transceiver will switch from CAN Active mode or CAN Listen-only mode to CAN Offline mode:

  CAN transceiver is in Normal and CMC = 00 or

  CAN mode is Reset or Standby or Sleep

The premise is that the CAN-bus has been inactive for at least $t_{to(silence)}$, the CAN transceiver will switch first to CAN Offline Bias mode and then to CAN Offline mode once the bus has been silent for $t_{to(silence)}$ when the CAN-bus has been inactive for less than $t_{to(silence)}$.

4.3 CAN Listen-only mode

CAN Listen-only mode allows the SIT1167Q to monitor bus activity while the transceiver is inactive, without influencing bus levels. This facility could be used by development tools that need to listen to the bus but do not need to transmit or receive data or for software-driven selective wake-up. Dedicated microcontrollers could be used for selective wake-up, providing an embedded low-power CAN engine designed to monitor the bus for potential wake-up events.

In Listen-only mode the CAN transmitter is disabled, reducing current consumption. The CAN receiver and CAN biasing remain active. This enables the host microcontroller to switch to a low-power mode in which an embedded CAN protocol controller remains active, waiting for a signal to wake up the microcontroller.

The CAN transceiver is in Listen-only mode when:

• the SIT1167Q is in Normal mode and CMC = 11

• the CAN transceiver will not leave Listen-only mode while TXD is LOW or CAN Active mode is selected with CMC = 01 while the voltage on V_{CAN} is below the 90 % undervoltage threshold.

4.4 CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL, the CAN bias voltage is derived from V1. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines. CAN Active mode is selected when CMC = 01 or 10. When CMC = 01, V_{CAN} undervoltage detection is enabled and the transceiver will go to CAN Offline or CAN Offline Bias mode when the voltage on V_{CAN} drops below the 90 % threshold. When CMC = 10, V_{CAN} undervoltage detection is disabled. The transmitter will remain active until the voltage on V1 drops below the V1 reset threshold (selected via bits V1RTC). The SBC will then switch to Reset mode and the transceiver will switch to CAN Offline or CAN Offline Bias mode.

The CAN transceiver is in Active mode when:

• the SIT1167Q is in Normal mode (MC = 111) and the CAN transceiver has been enabled by setting bits CMC in the CAN control register to 01 or 10

• if CMC = 01, the voltage on pin V_{CAN} is above the 90 % undervoltage threshold

• if CMC = 10, the voltage on pin V1 is above the V1 reset threshold

If pin TXD is held LOW when CAN Active mode is selected via bits CMC, the transceiver will not enter CAN Active mode but will switch to or remain in CAN Listen-only mode. It will remain in Listen-only mode until pin TXD goes HIGH in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state. In CAN Active mode, the CAN bias voltage is derived from V1.

5 CAN mode control

When the SIT1167Q is in Normal mode, the CAN transceiver operating mode (Active, Listen-only or Offline) can be selected via bits CMC in the CAN control register. When the SIT1167Q is in Standby or Sleep modes, the transceiver is forced to Offline or Offline Bias mode (depending on bus activity).

Table 4 CAN control register (address 20h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R		

Bit	Symbol	Access	Value	Description
1:0	CMC	R/W		CAN transceiver operating mode selection (available when SIT1167Q is in Normal mode; MC=111):
			00	Offline mode
			01	Active mode (V_{CAN} undervoltage detection is enabled)
			10	Active mode (V_{CAN} undervoltage detection is disabled)
			11	Listen-only mode

6 Transceiver status

The application can determine whether the CAN transceiver is ready to transmit/receive data or is disabled by reading the CAN Transceiver Status (CTS) bit.

Table 5 Transceiver status register (address 22h)

Bit	Symbol	Access	Value	Description
7	CTS	R	0	CAN transceiver not in Active mode
			1	CAN transceiver in Active mode
6:4	Reserved	R		
3	CBSS	R	0	CAN bus active (communication detected on bus)
			1	CAN bus inactive (for longer than $t_{to(silence)}$
2	Reserved	R		
1	VCS (1)	R	0	The output voltage on V1 is above the 90% threshold
			1	The output voltage on V1 is below the 90% threshold
0	CFS	R	0	No TXD dominant timeout event detected
			1	CAN transmitter disabled due to a TXD dominant timeout event

(1) Only active when CMC = 01.

7 Watchdog

The SIT1167Q contains a watchdog that supports three operating modes: Window, Timeout and Autonomous. Eight watchdog periods are supported, from 8ms to 4096ms. The watchdog period is programmed via bits NWP. The selected period is valid for both Window and Timeout modes. The default watchdog period is 128ms. A watchdog trigger event resets the watchdog timer. A watchdog trigger event is any valid write access to the Watchdog control register. If the watchdog mode or the watchdog period have changed as a result of the write access, the new values are immediately valid.

The watchdog mode is selected via bits WMC in the Watchdog control register. The SBC must be in Standby mode when the watchdog mode or period is changed. If Window mode is selected (WMC = 100), the watchdog will remain or switch Timeout mode until the SBC enters Normal mode.

Any attempt to change the watchdog operating mode or period (via WMC or NWP) while the SBC is in Normal mode will cause the SIT1167Q to switch to Reset mode. The reset source status bits (RSS = 10000, 'illegal watchdog mode control access' see **Table 3**) and a SPI failure (SPIF) event triggered, if enabled (SPIFE).

In Window mode when available only in SBC Normal mode, a watchdog trigger event within a closed watchdog window resets the watchdog timer.

In Timeout mode, the watchdog runs continuously and can be reset at any time within the timeout time by a watchdog trigger. Watchdog timeout mode can also be used for cyclic wake-up of the microcontroller.

In Autonomous mode, the watchdog can be off or in Timeout mode.

Table 6 Watchdog configuration

Operating/watchdog mode						
FNMC (Forced Normal mode control)		0	0	0	0	1
SDMC (Software Development mode control)		x	x	0	1	x
WMC (watchdog mode control)		100 (Window)	010 (Timeout)	001 (Autonomous)	001 (Autonomous)	n.a.
SBC Operating Mode	Normal mode	Window	Timeout	Timeout	Off	Off
	Standby mode (RXD HIGH) (1)	Timeout	Timeout	Off	Off	Off
	Standby mode (RXD LOW) (1)	Timeout	Timeout	Timeout	Off	Off
	Sleep mode	Timeout	Timeout	Off	Off	Off
	Other modes	Off	Off	Off	Off	Off

(1) RXD LOW signals a pending wake-up.

Table 7 Watchdog control register (address 00h)

Bit	**Symbol**	**Access**	**Value**	**Description**
7:5	WMC	R/W		Watchdog mode control
			001 (1)	Autonomous mode
			010 (2)	Timeout mode
			100 (3)	Window mode
4	Reserved	R		
3:0	NWP	R/W		Nominal watchdog period
			1000	8ms
			0001	16ms
			0010	32ms
			1011	64ms
			0100 (2)	128ms

Bit	Symbol	Access	Value	Description
			1101	256ms
			1110	1024ms
			0111	4096ms

(1) Default value if SDMC=1
(2) Default value.
(3) Selected in Standby mode but only activated when the SBC switches to Normal mode.

Two operating modes have a major impact on the operation of the watchdog: Forced Normal mode and Software Development mode (Software Development mode is provided for test purposes and is not an SBC operating mode; the SIT1167Q can be in any mode with Software Development mode enabled. These modes are enabled and disabled via bits FNMC and SDMC respectively in the SBC configuration control register (see **Table 8**). Note that this register is located in the non-volatile memory area. In Forced Normal mode (FNM), the watchdog is completely disabled. In Software Development mode (SDM), the watchdog can be disabled or activated for test purposes.

Table 8 SBC configuration control register (address 74h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R		Watchdog mode control
5:4	V1RTSUC	R/W		V1 reset threshold (defined by bit V1RTC) at start-up
			00(1)	V1 undervoltage detection at 90% of nominal value at start-up (V1RTC=00)
			01	V1 undervoltage detection at 80% of nominal value at start-up (V1RTC=01)
			10	V1 undervoltage detection at 70% of nominal value at start-up (V1RTC=10)
			11	V1 undervoltage detection at 60% of nominal value at start-up (V1RTC=11)
3	FNMC	R/W		Forced Normal mode control:
			0	Forced Normal mode disabled
			1(1)	Forced Normal mode disabled
2	SDMC	R/W		Software Development mode control:
			0(1)	Software Development mode disabled
			1	Software Development mode enabled
1	Reserved	R		
0	SLPC	R/W		Sleep mode:
			0(1)	The SBC supports Sleep mode

Bit	Symbol	Access	Value	Description
			1	Sleep mode commands will be ignored

(1) Factory preset value.

Information on the status of the watchdog is available from the Watchdog status register (**Table 9**). This register also indicates whether Forced Normal and Software Development modes are active.

Table 9 Watchdog status register (address 05h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R		
3	FNMS	R	0	SBC is not in Forced Normal mode
			1	SBC is in Forced Normal mode
2	SDMS	R	0	SBC is not in Software Development mode
			1	SBC is on Software Development mode
1:0	WDS	R		Watchdog status:
			00	Watchdog is off
			01	Watchdog is in first half of window
			10	Watchdog is in second half of window
			11	reserved

7.1 Software Development mode

Software Development mode is provided to simplify the software design process. When Software Development mode is enabled, the watchdog starts up in Autonomous mode (WMC = 001) and is inactive after a system reset, overriding the default value (see **Table 9**). The watchdog is always off in Autonomous mode if Software Development mode is enabled (SDMC = 1; see **Table 6**).

Software can be run without a watchdog in Software Development mode. However, it is possible to activate and deactivate the watchdog for test purposes by selecting Window or Timeout mode via bits WMC while the SBC is in Standby mode (note that Window mode will only be activated when the SBC switches to Normal mode). Software Development mode is activated via bits SDMC in non-volatile memory (see **Table 8**).

7.2 Window mode

The watchdog runs continuously in Window mode. The watchdog will be in Window mode if WMC = 100 and the SIT1167Q is in Normal mode. In Window mode, the watchdog can only be triggered during the second half of the watchdog period.

If the watchdog overflows, or is triggered in the first half of the watchdog period (before $t_{trig(wd)1}$), a system reset is performed. After the system reset, the reset source (either ‘watchdog triggered too early’ or ‘watchdog overflow’) can be read via the reset source status bits (RSS) in the Main Status register.

If the watchdog is triggered in the second half of the watchdog period (after $t_{trig(wd)1}$ but before $t_{trig(wd)2}$), the watchdog timer is restarted.

7.3 Timeout mode

The watchdog runs continuously in Timeout mode. The watchdog will be in Timeout mode if WMC = 010 and the SIT1167Q is in Normal, Standby or Sleep mode. The watchdog will also be in Timeout mode if WMC = 100 and the SIT1167Q is in Standby or Sleep mode. If Autonomous mode is selected (WMC = 001), the watchdog will be in Timeout mode if one of the conditions for Timeout mode has been satisfied.

In Timeout mode, the watchdog timer can be reset at any time by a watchdog trigger. If the watchdog overflows, a watchdog failure event (WDF) is captured. If a WDF is already pending when the watchdog overflows, a system reset is performed. In Timeout mode, the watchdog can be used as a cyclic wake-up source for the microcontroller when the SIT1167Q is in Standby or Sleep mode. In Sleep mode, a watchdog overflow generates a wake-up event.

When the SBC is in Sleep mode with watchdog Timeout mode selected, a wake-up event s generated after the nominal watchdog period (NWP). If bit WDF is set, RXD is forced LOW and V1 is turned on. The application software can then clear the WDF bit and trigger the watchdog before it overflows.

7.4 Autonomous mode

Autonomous mode is selected when WMC = 001. When Autonomous mode is selected, the watchdog will be in Timeout mode if the SBC is in Normal mode or Standby mode with RXD LOW, provided Software Development mode has been disabled (SDMC = 0). Otherwise the watchdog will be off.

In Autonomous mode, the watchdog will not be running when the SBC is in Standby (RXD HIGH) or Sleep mode. If a wake-up event is captured, pin RXD is forced LOW to signal the event and the watchdog is automatically restarted in Timeout mode. If the SBC was in Sleep mode when the wake-up event was captured, it switches to Standby mode.

Table 10 Watchdog status in Autonomous mode

SIT1167Q operating mode	**Watchdog status**	
	SDMC=0	**SDMC=1**
Normal	Timeout mode	Off
Standby; RXD HIGH	Off	Off
Sleep	Off	Off
Any other mode	Off	Off
Standby; RXD LOW	Timeout mode	Off

8 System reset

When a system reset occurs, the SBC switches to Reset mode and initiates a process that generates a low-level pulse on pin RSTN.

8.1 Characteristics of pin RSTN

Pin RSTN is a bidirectional open drain low side driver with integrated pull-up resistance, as shown in **Figure 5**. The input reset pulse width must be at least $t_{w(rst)}$. With this configuration, the SBC can detect the pin being pulled down externally, e.g. by the microcontroller.

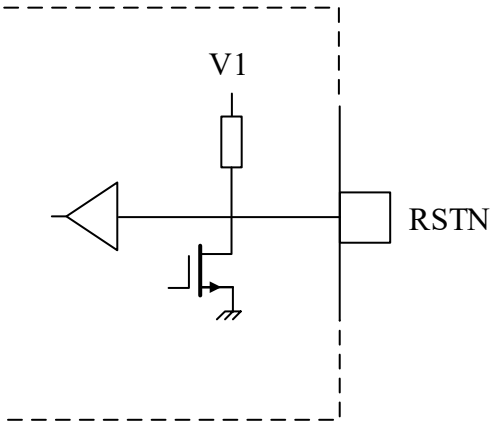


Figure 5 RSTN internal pin configuration

8.2 Selecting the output reset pulse width

The duration of the output reset pulse is selected via bits RLC in the Start-up control register (**Table 11**). The SBC distinguishes between a cold start and a warm start. A cold start is performed if the reset event was combined with a V1 undervoltage event (power-on reset, reset during Sleep mode, over-temperature reset, V1 undervoltage before entering or while in Reset mode). The output reset pulse width for a cold start is determined by the setting of bits RLC.

If any other reset event occurs without a V1 undervoltage (external reset, watchdog failure, watchdog change attempt in Normal mode, illegal Sleep mode command) the SBC uses the shortest reset length ($t_{w(rst)}$ = 1 ms to 1.5 ms). This is called a warm start of the microcontroller.

Table 11 Start-up control register (address 73h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R		
5:4	RLC	R/W		RSTN output reset pulse width:
			00 (1)	$t_{w(rst)}$=20ms to 25ms
			01	$t_{w(rst)}$=10ms to 12.5ms
			10	$t_{w(rst)}$=3.6ms to 5ms
			11	$t_{w(rst)}$=1ms to 1.5ms
3	VEXTSUC	R/W		INH start-up control:

Bit	Symbol	Access	Value	Description
			0	Bits VEXTC set to 00 at power-up
			1	Bits VEXTC set to 11 at power-up
2:0	Reserved	R		

(1) Factory preset value.

8.3 Reset sources

The following events will cause the SIT1167Q to switch to Reset mode:

- V_{V1} drops below the selected V1 undervoltage threshold defined by bits V1RTC
- via Off mode after an MTPNV programming cycle has been completed
- pin RSTN is pulled down externally
- the watchdog overflows in Window mode
- the watchdog is triggered too early in Window mode (before $t_{trig(wd)1}$)
- the watchdog overflows in Timeout mode with WDF = 1 (watchdog failure pending)
- an attempt is made to reconfigure the Watchdog control register while the SBC is in Normal mode
- the SBC leaves Off mode
- local or CAN bus wake-up in Sleep mode
- diagnostic wake-up in Sleep mode
- the SBC leaves Overtemp mode
- illegal Sleep mode command received

9 Global temperature protection

The temperature of the SIT1167Q is monitored continuously, except in Sleep and Off modes. The SBC switches to Overtemp mode if the temperature exceeds the overtemperature protection activation threshold, $T_{th(act)otp}$. In addition, pin RSTN is driven LOW, V1 and the CAN transceiver are switched off. When the temperature drops below the overtemperature protection release threshold, $T_{th(rel)otp}$, the SBC switches to Standby mode via Reset mode. In addition, the SIT1167Q provides an overtemperature warning. When the IC temperature rises about the overtemperature warning threshold ($T_{th(warn)otp}$), status bit OTWS is set and an overtemperature warning event is captured (OTW = 1).

10 Power supplies

10.1 Battery supply voltage (V_{BAT})

The internal circuitry is supplied from the battery via pin BAT. The device needs to be protected against negative supply voltages, e.g. by using an external series diode. If V_{BAT} falls below the power-off detection

threshold, $V_{th(det)poff}$, the SBC switches to Off mode. However, the microcontroller supply voltage (V1) remains active until VBAT falls below 2 V.

The SBC switches from Off mode to Reset mode $t_{startup}$ after the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$. Power-on event status bit PO is set to 1 to indicate the SIT1167Q has powered up and left Off mode (see **Table 18**).

10.2 Low-drop voltage supply for 5 V microcontroller (V1)

V1 is intended to supply the microcontroller and the internal CAN transceiver and delivers up to 150mA at 5V. The output voltage on V1 is monitored. A system reset is generated if the voltage on V1 drops below the selected undervoltage threshold (60%, 70%, 80% or 90% of the nominal V1 output voltage, selected via V1RTC in the V1 and INH control register; see **Table 12**). When V1 is turned off, the voltage of V1 will drop rapidly to GND through the internal pull-down circuits.

The internal CAN transceiver consumes 50mA (max) when the bus is continuously dominant, leaving 100mA available for the external load on pin V1. In practice, the typical current consumption of the CAN transceiver is lower (≈25mA), depending on the application, leaving more current available for the load.

The default value of the undervoltage threshold at power-up is determined by the value of bits V1RTSUC in the SBC configuration control register (**Table 8**). The SBC configuration control register is in non-volatile memory, allowing the user to define the undervoltage threshold (V1RTC) at start-up.

In addition, an undervoltage warning (a V1U event; see Section 7.10) is generated if the voltage on V1 falls below 90% of the nominal value (and V1U event detection is enabled, V1UE=1; see **Table 23**). This information can be used as a warning, when the 60%, 70% or 80% threshold is selected, to indicate that the level on V1 is outside the nominal supply range. The status of V1, whether it is above or below the 90% undervoltage threshold, can be read via bit V1S in the Supply voltage status register (**(1)** Default value at power-up defined by setting of bits VEXTSUC (see **Table 11**).
(2) Default value at power-up defined by setting of bits V1RTSUC (see **Table 8**).

Table 13).

Table 12 V1 and INH control register (address 10h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R		
3:2	VEXTC (1)	R/W		INH configuration:
			00	INH off in all modes
			01	INH on in Normal mode
			10	INH on in Normal, Standby and Reset modes
			11	INH on in Normal, Standby, Sleep and Reset modes
1:0	V1RTC (2)	R/W		Set V1 reset threshold:

Bit	Symbol	Access	Value	Description
			00	Reset threshold set to 90% of V1 nominal output voltage
			01	Reset threshold set to 80% of V1 nominal output voltage
			10	Reset threshold set to 70% of V1 nominal output voltage
			11	Reset threshold set to 60% of V1 nominal output voltage

(1) Default value at power-up defined by setting of bits VEXTSUC (see **Table 11**).

(2) Default value at power-up defined by setting of bits V1RTSUC (see **Table 8**).

Table 13 Supply voltage status register (address 1Bh)

Bit	Symbol	Access	Value	Description
7:1	reserved	R		
0	V1S	R		V1 status:
			0 (1)	V1 output voltage above 90% undervoltage threshold
			1	V1 output voltage below 90% undervoltage threshold

(1) Default value at power-up.

11 High voltage output

Depending on the device version, pin 7 is a high voltage output (INH).

In the SIT1167Q, the INH pin can be used to control external devices, such as voltage regulators. Depending on the setting of bits VEXTC, pin INH will either be disabled (to disable external devices) or at a battery-related HIGH level (to enable external devices) in selected SBC operating modes (see **Table 8**). To ensure external devices are not disabled due to an overtemperature event, pin INH does not change state when the SBC switches to Overtemp mode.

The default value of VEXTC at power-on is defined by bits VEXTSUC in non-volatile memory.

In contrast to pin INH is disabled when the SBC switches to Overtemp mode.

12 CAN standard wake-up

If the CAN transceiver is in Offline mode and CAN wake-up is enabled (CWE = 1), the SIT1167Q will monitor the bus for a wake-up pattern.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. A dominant-recessive-dominant wake-up pattern must be transmitted on the CAN bus within the wake-up timeout time ($t_{to(wake)}$) to pass the wake-up filter and trigger a wake-up event (see **Figure 6**; note that additional pulses may occur between the recessive/dominant phases). The recessive and dominant phases must last at

least $t_{wake(busrec)}$ and $t_{wake(busdom)}$, respectively.

When a valid CAN wake-up pattern is detected on the bus, wake-up bit CW in the Transceiver event status register is set (see **Table 20**) and pin RXD is driven LOW. If the SBC was in Sleep mode when the wake-up pattern was detected, V1 is enabled to supply the microcontroller and the SBC switches to Standby mode via Reset mode.

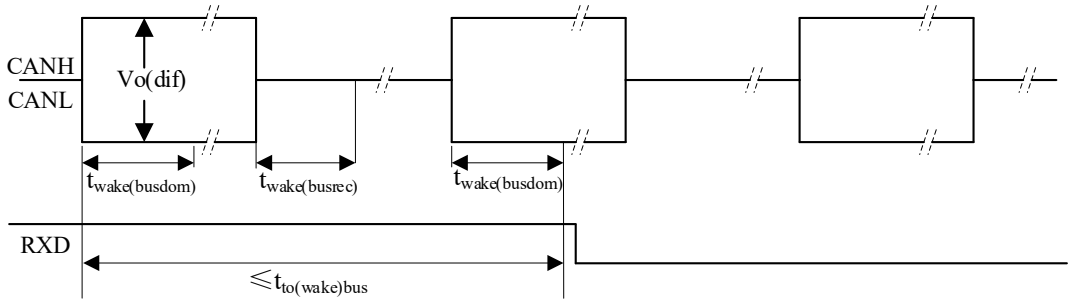


Figure 6 CAN wake-up timing

13 Local wake-up via WAKE pin

Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register (see **Table 25**). A wake-up event is triggered by a LOW-to-HIGH (if WPRE = 1) and/or a HIGH-to-LOW (if WPFE = 1) transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit. In applications that don't make use of the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND to ensure optimal EMI performance.

While the SBC is in Normal mode, the status of the voltage on pin WAKE can always be read via bit WPVS. Otherwise, WPVS is only valid if local wake-up is enabled (WPRE = 1 and/or WPFE = 1).

Table 14 WAKE status register (address 4Bh)

Bit	Symbol	Access	Value	Description
7:2	Reserved	R		
1	WPVS	R		WAKE pin status:
			0	Voltage on WAKE pin below switching threshold ($V_{th(sw)}$)
			1	Voltage on WAKE pin above switching threshold ($V_{th(sw)}$)
0	Reserved	R		

14 CAN fail-safe features

14.1 TXD dominant timeout

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in CAN

Active Mode. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 4.4 kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure event is captured (CF = 1; see **Table 20**), if enabled (CFE = 1; see **Table 24**). In addition, the status of the TXD dominant timeout can be read via the CFS bit in the Transceiver status register and bit CTS is cleared.

14.2 Pull-up on TXD pin

Pin TXD has an internal pull-up towards V1 to ensure a safe defined recessive driver state in case the pin is left floating.

14.3 V_{CAN} undervoltage event

When CMC = 01, a CAN failure event is captured (CF = 1) and status bit VCS is set to 1 when the supply to the CAN transceiver (V_{CAN}) falls below 90 % of its nominal value (assuming CAN failure detection is enabled; CFE = 1).

14.4 Loss of power at pin BAT

A loss of power at pin BAT has no influence on the bus lines or on the microcontroller. No reverse currents will flow from the bus.

15 Wake-up and interrupt event diagnosis via pin RXD

Wake-up and interrupt event diagnosis in the SIT1167Q is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the event status registers (**Table 18** to **Table 20**) and is signaled on pin RXD, if enabled.

A distinction is made between regular wake-up events and interrupt events (at least one regular wake-up source must be enabled to allow the SIT1167Q to switch to Sleep mode).

Table 15 Regular events

Symbol	Event	Power-on	Description
CW	CAN wake-up	disabled	a CAN wake-up event was detected while the transceiver was in CAN Offline mode.
WPR	rising edge on WAKE pin	disabled	a rising-edge wake-up was detected on pin WAKE
WPF	falling edge on WAKE pin	disabled	a falling-edge wake-up was detected on pin WAKE

Table 16 Diagnostic events

Symbol	Event	Power-on	Description
PO	power-on	always enabled	the SIT1167Q has exited Off mode (after battery power has been restored/connected)
OTW	overtemperature warning	disabled	the IC temperature has exceeded the overtemperature warning threshold (not in Sleep mode)
SPIF	SPI failure	disabled	SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal WMC, NWP or MC code or attempted write access to locked register (not in Sleep mode)
WDF	watchdog failure	always enabled	watchdog overflow in Timeout mode; when the watchdog overflows in Timeout mode, a system reset is only performed if a WDF is already pending (WDF = 1)
V1U	V1 undervoltage	disabled	voltage on V1 has dropped below the 90 % undervoltage threshold when V1 is active (event is not captured in Sleep mode because V1 is off). V1U event capture is independent of the setting of bits V1RTC.
CBS	CAN-bus silence	disabled	no activity on CAN bus for $t_{to(silence)}$ (detected only when CBSE = 1 while bus active)
CF	CAN failure	disabled	one of the following CAN failure events detected: - CAN transceiver deactivated due to a V1 undervoltage - CAN transceiver deactivated due to a dominant clamped TXD (not in Sleep mode)

PO and WDF interrupts are always captured. Wake-up and interrupt detection can be enabled/disabled for the remaining events individually via the event capture enable registers (**Table 22** to **Table 24**).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in CAN Offline mode with V1 active (SBC Normal or Standby mode), pin RXD is forced LOW to indicate that a wake-up or interrupt event has been detected. If the SIT1167Q is in sleep mode when the event occurs, the microcontroller supply, V1, is activated and the SBC switches to Standby mode (via Reset mode).

The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register (**Table 17**), is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, supply, transceiver or WAKE pin) and then query the relevant table (**Table 18**, **Table 19**, **Table 20** or **Table 21** respectively).

After the event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant bit (writing 0 will have no effect). A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits.

It is strongly recommended to clear only the status bits that were set to 1 when the status registers were last

read. This precaution ensures that events triggered just before the write access are not lost.

15.1 Interrupt/wake-up delay

If interrupt or wake-up events occur very frequently while the transceiver is in CAN Offline mode, they can have a significant impact on the software processing time (because pin RXD is repeatedly driven LOW, requiring a response from the microcontroller each time an interrupt/wake-up is generated). The SIT1167Q incorporates an event delay timer to limit the disturbance to the software.

When one of the event capture status bits is cleared, pin RXD is released (HIGH) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after $t_{d(event)}$, pin RXD goes LOW again to alert the microcontroller.

In this way, the microcontroller is interrupted once to process a number of events rather than several times to process individual events.

If all events are cleared while the timer is running, RXD remains HIGH after the timer expires, since there are no pending events. The event capture registers can be read at any time.

The event capture delay timer is stopped immediately when pin RSTN goes low (triggered by a HIGH-to-LOW transition on the pin). RSTN is driven LOW when the SBC enters Reset, Sleep, Overtemp and Off modes. A pending event is signaled on pin RXD when the SBC enters Sleep mode.

15.2 Sleep mode protection

The wake-up event capture function is critical when the SIT1167Q is in Sleep mode, because the SBC will only leave Sleep mode in response to a captured wake-up event. To avoid potential system deadlocks, the SBC distinguishes between regular and diagnostic events. Wake-up events (via the CAN bus or the WAKE pin) are classified as regular events; diagnostic events signal failure/error conditions or state changes. At least one regular wake-up event must be enabled before the SIT1167Q can switch to Sleep mode. Any attempt to enter Sleep mode while all regular wake-up events are disabled will trigger a system reset.

Another condition that must be satisfied before the SIT1167Q can switch to Sleep mode is that all event status bits must be cleared. If an event is pending when the SBC receives a Sleep mode command (MC = 001), it will immediately switch to Reset mode. This condition applies to both regular and diagnostic events.

Sleep mode can be permanently disabled in applications where, for safety reasons, the supply voltage to the host controller must never be cut off. Sleep mode is permanently disabled by setting the Sleep control bit (SLPC) in the SBC configuration register (see **Table 8**) to 1. This register is located in the non-volatile memory area of the device. When SLPC = 1, a Sleep mode SPI command (MC = 001) will trigger an SPI failure event instead of a transition to Sleep mode.

15.3 Event status and event capture registers

After an event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant status bit (writing 0 will have no effect).

Table 17 Global event status register (address 60h)

Bit	Symbol	Access	Value	Description
7:4	Reserved	R		
3	WPE	R	0	No pending WAKE pin event
			1	WAKE pin event pending at address 64h
2	TRXE	R	0	No pending transceiver event
			1	Transceiver event pending at address 63h
1	SUPE	R	0	No pending supply event
			1	Supply event pending at address 62h
0	SYSE	R	0	No pending system event
			1	System event pending at address 61h

Table 18 System event status register (address 61h)

Bit	Symbol	Access	Value	Description
7:5	Reserved	R		
4	PO	R/W	0	No recent power-on
			1	The SIT1167Q has left Off mode after power-on
3	Reserved	R		
2	OTW	R/W	0	Overtemperature not detected
			1	The global chip temperature has exceeded the overtemperature warning threshold ($T_{th(warn)otp}$)
1	SPIF	R/W	0	No SPI failure detected
			1	SPI failure detected
0	WDF	R/W	0	no watchdog failure event captured
			1	Watchdog failure event captured

Table 19 Supply event status register (address 62h)

Bit	Symbol	Access	Value	Description
7:1	Reserved	R		
0	V1U	R/W	0	No V1 undervoltage event captured
			1	V1 undervoltage event captured

Table 20 Transceiver event status register (address 63h)

Bit	Symbol	Access	Value	Description
7:5	Reserved	R		

Bit	Symbol	Access	Value	Description
4	CBS	R/W	0	CAN bus active
			1	No activity on CAN bus for $t_{to(silence)}$
3:2	Reserved	R		
1	CF	R/W	0	No CAN failure detected
			1	(CMC=01 & CAN transceiver deactivated due to V1 undervoltage) OR dominant clamped TXD
0	CW	R/W	0	No CAN wake-up event detected
			1	CAN wake-up event detected while the transceiver is in CAN Offline Mode

Table 21 WAKE pin event capture status register (address 64h)

Bit	Symbol	Access	Value	Description
7:2	Reserved	R		
1	WPR	R/W	0	No rising edge detected on WAKE pin
			1	Rising edge detected on WAKE pin
0	WPF	R/W	0	No falling edge detected on WAKE pin
			1	Falling edge detected on WAKE pin

Table 22 System event capture status register (address 04h)

Bit	Symbol	Access	Value	Description
7:3	Reserved	R		
2	OTWE	R/W		Overtemperature warning event capture:
			0	Overtemperature warning disabled
			1	Overtemperature warning enabled
1	SPIFE	R/W		SPI failure detection:
			0	SPI failure detection disabled
			1	SPI failure detection enabled
0	Reserved	R		

Table 23 Supply event capture enable register (address 1Ch)

Bit	Symbol	Access	Value	Description
7:1	Reserved	R		
0	V1UE	R/W		V1 undervoltage detection:
			0	V1 undervoltage detection disabled

Bit	Symbol	Access	Value	Description
			1	V1 undervoltage detection enabled

Table 24 Transceiver event capture enable register (address 23h)

Bit	Symbol	Access	Value	Description
7:5	Reserved	R		
4	CBSE	R/W		CAN bus silence detection
			0	CAN bus silence detection disabled
			1	CAN bus silence detection enabled
3:2	Reserved	R		
1	CFE	R/W		CAN failure detection
			0	CAN failure detection disabled
			1	CAN failure detection enabled
0	CWE	R/W		CAN wake-up detection:
			0	CAN wake-up detection disabled
			1	CAN wake-up detection enabled

Table 25 WAKE pin event capture enable register (address 4Ch)

Bit	Symbol	Access	Value	Description
7:2	Reserved	R		
1	WPRE	R/W		Rising-edge detection on WAKE pin:
			0	Rising-edge detection on WAKE pin disabled
			1	Rising-edge detection on WAKE pin enabled
0	WPFE	R/W		Falling-edge detection on WAKE pin:
			0	Falling-edge detection on WAKE pin disabled
			1	Falling-edge detection on WAKE pin enabled

16 Non-volatile SBC configuration

The SIT1167Q contains Multiple Time Programmable Non-Volatile (MTPNV) memory cells that allow some of the default device settings to be reconfigured. The MTPNV memory address range is from 73h to 74h. An overview of the MTPNV registers is given in **Table 26**.

Table 26 Overview of MTPNV registers

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
73h	Start-up control	Reserved		RLC		VEXTSUC	Reserved		

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
74h	SBC configuration control	Reserved		V1RTSUC		FNMC	SDMC	Reserved	SLPC

16.1 Programming MTPNV cells

The SIT1167Q must be in Forced Normal mode and the MTPNV cells must contain the factory preset values before the non-volatile memory can be reprogrammed. The SIT1167Q will switch to Forced Normal mode after a reset event (e.g. pin RSTN LOW) when the MTPNV cells contain the factory preset values (since FNMC = 1).

The factory presets may need to be restored before reprogramming can begin (see Section 7.11.2). When the factory presets have been restored, a system reset is generated automatically and SIT1167Q switches to Forced Normal mode. This ensures that the programming cycle cannot be interrupted by the watchdog.

Programming of the non-volatile memory registers is performed in two steps. First, the required values are written to addresses 73h and 74h. In the second step, reprogramming is confirmed by writing the correct CRC value to the MTPNV CRC control register. The SBC starts reprogramming the MTPNV cells as soon as the CRC value has been validated. If the CRC value is not correct, reprogramming is aborted. On completion, a system reset is generated to indicate that the MTPNV cells have been reprogrammed successfully. Note that the MTPNV cells cannot be read while they are being reprogrammed.

After an MTPNV programming cycle has been completed, the non-volatile memory is protected from being overwritten via a standard SPI write operation.

The MTPNV cells can be reprogrammed a maximum of 200 times ($N_{cy(W)MTP}$). Bit NVMPS in the MTPNV status register (**Table 27**) indicates whether the non-volatile cells can be reprogrammed. This register also contains a write counter, WRCNTS, that is incremented each time the MTPNV cells are reprogrammed (up to a maximum value of 111111; there is overflow; performing a factory reset also increments the counter). This counter is provided for information purposes only; reprogramming will not be rejected when it reaches its maximum value.

An error correction code status bit, ECCS, is set to indicate that the CRC check mechanism in the SBC has detected a single bit failure in non-volatile memory. If more than one bit failure is detected, the SBC will not restart after MTPNV reprogramming. Check the ECCS flag at the end of the production cycle to verify the content of non-volatile memory. When this flag is set, it indicates a device or ECU failure.

Table 27 MTPNV status register (address 70h)

Bit	Symbol	Access	Value	Description
7:2	WRCNTS	R		Write counter status:

Bit	Symbol	Access	Value	Description
			xxxxxx	Contains the number of times the MTPNV cells were reprogrammed
1	ECCS	R		Error correction code status:
			0	No bit failure detected in non-volatile memory
			1	Bit failure detected and corrected in non-volatile memory
0	NVMPS	R		Non-volatile memory programming status:
			0	MTPNV memory cannot be overwritten
			1(1)	MTPNV memory is ready to be reprogrammed

(1) Default value at power-up.

16.1.1 Calculating the CRC value for MTP programming

The cyclic redundancy check value stored in bits CRCC in the MTPNV CRC control register is calculated using the data written to registers 73h and 74h.

Table 28 MTPNV CRC control register (address 75h)

Bit	Symbol	Access	Value	Description
7:0	CRCC	W		CRC control data

The CRC value is calculated using the data representation shown in **Figure 7** and the modulo-2 division with the generator polynomial: $X^8 + X^5 + X^3 + X^2 + X + 1$. The result of this operation must be bitwise inverted.

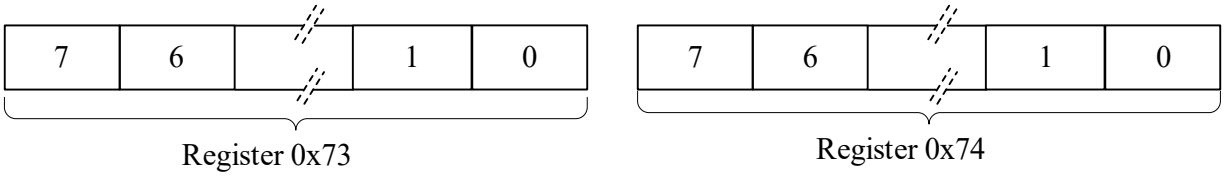


Figure 7 Data representation for CRC calculation

The following parameters can be used to calculate the CRC value (e.g. via the Autosar method):

Table 29 Parameters for CRC coding

Parameter	Value
CRC result width	8 bits
Polynomial	2Fh
Initial value	FFh
Input data reflected	no
Result data reflected	no

Parameter	Value
XOR value	FFh

Alternatively, the following algorithm can be used:

data = 0 // unsigned byte

crc = FFh

for i = 0 to 1

    data = content of address (73h+i) EXOR crc

    for j = 0 to 7

        if data ≥ 128

            data = data * 2 // shift left by 1

            data = data EXOR 2Fh

        else

            data = data * 2 // shift left by 1

    next j

    crc = data

next i

crc = crc EXOR FFh

16.2 Restoring factory preset values

Factory preset values are restored if the following conditions apply for at least $t_{d(MTPNV)}$ during power-up:

• pin RSTN is held LOW

• CANH is pulled up to V_{BAT}

• CANL is pulled down to GND

After the factory preset values have been restored, the SBC performs a system reset and enters Forced normal Mode. Since the CAN bus is clamped dominant, pin RXDC is forced LOW. During the factory preset restore process, this pin is forced HIGH; a falling edge on this pin caused by bit PO being set after power-on then clearly indicates that the process has been completed.

Note that the write counter, WRCNTS, in the MTPNV status register is incremented every time the factory presets are restored.

17 Device ID

A byte is reserved at address 7Eh for a SIT1167Q identification code.

Table 30 Identification register (address 7Eh)

Bit	Symbol	Access	Value	Description
7:0	IDS	R	D8h	Device identification code – SIT1167Q

18 Lock control register

Sections of the register address area can be write-protected to protect against unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the SIT1167Q updating status registers etc.

Table 31 Lock control register (address 0Ah)

Bit	Symbol	Access	Value	Description
7	Reserved	R		Cleared for future use
6	LK6C	R/W		Lock control 6: address area 68h to 6Fh
			0	SPI write-access enabled
			1	SPI write-access disabled
5	LK5C	R/W		Lock control 5: address area 50h to 5Fh
			0	SPI write-access enabled
			1	SPI write-access disabled
4	LK4C	R/W		Lock control 4: address area 40h to 4Fh – WAKE pin control
			0	SPI write-access enabled
			1	SPI write-access disabled
3	LK3C	R/W		Lock control 3: address area 30h to 3Fh
			0	SPI write-access enabled
			1	SPI write-access disabled
2	LK2C	R/W		Lock control 2: address area 20h to 2Fh – transceiver control
			0	SPI write-access enabled
			1	SPI write-access disabled
1	LK1C	R/W		Lock control 1: address area 10h to 1Fh – regulator control
			0	SPI write-access enabled
			1	SPI write-access disabled
0	LK0C	R/W		Lock control 0: address area 06h to 09h – general purpose memory
			0	SPI write-access enabled

Bit	Symbol	Access	Value	Description
			1	SPI write-access disabled

19 General purpose memory

SIT1167Q allocates 4 bytes of RAM as general-purpose registers for storing user information. The general-purpose registers can be accessed via the SPI at address 06h to 09h.

20 SPI

20.1 Introduction

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

• SCSN: SPI chip select; active LOW

• SCK: SPI clock; default level is LOW due to low-power concept (pull-down)

• SDI: SPI data input

• SDO: SPI data output; floating when pin SCSN is HIGH

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the

rising edge, as illustrated in **Figure 8**.

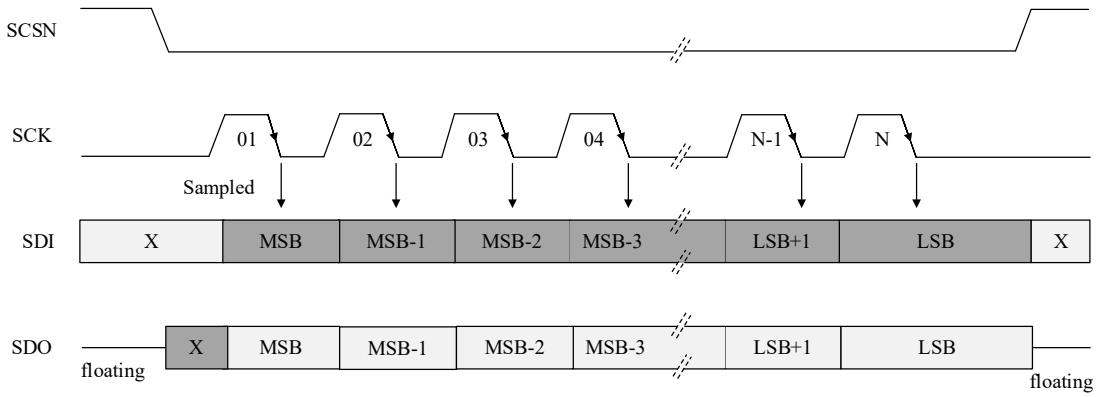


Figure 8 SPI timing protocol

The SPI data in the SIT1167Q is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 7-bit address. Two bytes must be transmitted to the SBC for a single register write operation. The first byte contains the 7-bit address along with a ‘read-only’ bit (the LSB). The read-only bit must be 0 to indicate a write operation (if this bit is 1, a read operation is assumed and any data on the SDI pin is ignored). The

second byte contains the data to be written to the register.

24- and 32-bit read and write operations are also supported. The register address is automatically incremented, once for a 24-bit operation and twice for a 32-bit operation, as illustrated in **Figure 9**.

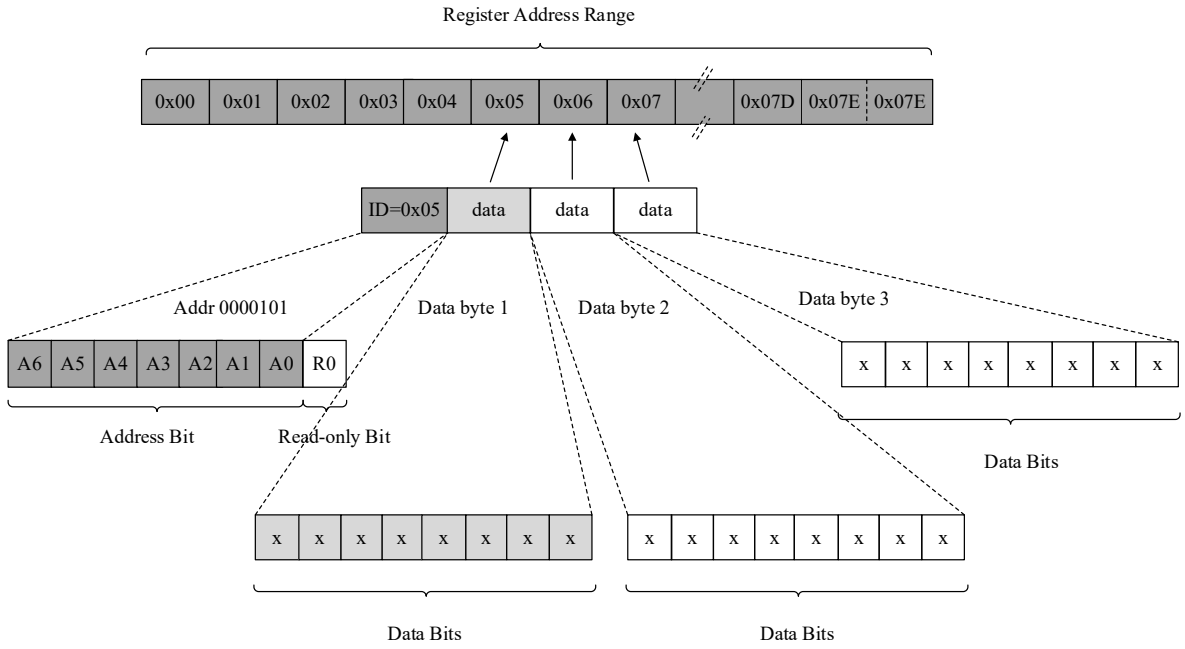


Figure 9 SPI data structure for a write operation (16-, 24- or 32-bit)

During an SPI data read or write operation, the contents of the addressed register(s) is returned via pin SDO.

The SIT1167Q tolerates attempts to write to registers that don't exist. If the available address space is exceeded during a write operation, the data above the valid address range is ignored (without generating an SPI failure event).

During a write operation, the SIT1167Q monitors the number of SPI bits transmitted. If the number recorded is not 16, 24 or 32, then the write operation is aborted and an SPI failure event is captured (SPIF = 1).

If more than 32 bits are clocked in on pin SDI during a read operation, the data stream on SDI is reflected on SDO from bit 33 onwards.

21 Register map

Table 32 Register map

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x00	Watchdog control	WMC			Reserved	NWP			
0x01	Mode control	Reserved					MC		
0x02	Fail-safe control	Reserved					LHC	RCC	
0x03	Main status	Reserved	OTWS	NMS	RSS				
0x04	System event enable	Reserved					OTWE	SPIFE	Reserved
0x05	Watchdog status	Reserved				FNMS	SDMS	WDS	
0x06	Memory 0	GPM [7:0]							
0x07	Memory 1	GPM [15:8]							
0x08	Memory 2	GPM [23:16]							
0x09	Memory 3	GPM [31:24]							
0x0A	Lock control	Reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C

Table 33 Overview of regulator control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x10	Regulator control	Reserved (1)				VEXTC		V1RTC	
0x1B	Supply status	Reserved							V1S
0x1C	Supply event enable	Reserved							V1UE

(1) Reserved bits can be read and overwritten without affecting device functionality; default value at power-up is 00 (other reserved bits always return 0).

Table 34 Overview of WAKE pin control and status registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x4B	WAKE pin status	Reserved						WPVS	Reserved
0x4C	WAKE pin enable	Reserved						WPRE	WPFE

Table 35 Overview of event capture registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x60	Global event status	Reserved				WPE	TRXE	SUPE	SYSE
0x61	System event status	Reserved			PO	Reserved	OTW	SPIF	WDF

0x62	Supply event status	Reserved				V1U
0x63	Transceiver event status	Reserved	CBS	Reserved	CF	CW
0x64	WAKE pin event status	Reserved			WPR	WPF

Table 36 Overview of MTPNV status register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x70	MTPNV status	WRCNTS						ECCS	NVMPS

Table 37 Overview of Start-up control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x73	Start-up control	Reserved		RLC		VEXTSUC	Reserved		

Table 38 Overview of SBC configuration control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x74	SBC configuration control	Reserved		V1RTSUC		FNMC	SDMC	Reserved	SLPC

Table 39 Overview of CRC control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x75	MTPNV CRC control	CRCC [7:0]							

Table 40 Overview of Identification register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x7E	Identification	IDS [7:0]							

21.1 Register configuration in SIT1167Q operating modes

A number of register bits may change state automatically when the SIT1167Q switches from one operating mode to another. This is particularly evident when the SIT1167Q switches to Off mode. These changes are summarized in **Table 41**. If an SPI transmission is in progress when the SIT1167Q changes state, the transmission is ignored (automatic state changes have priority).

Table 41 Register bit settings in SIT1167Q operating modes

Symbol	Off (power-on default)	Standby	Normal	Sleep	Overtempt	Reset
CBS	0	No change	No change	No change	No change	No change
CBSE	0	No change	No change	No change	No change	No change

Symbol	Off (power-on default)	Standby	Normal	Sleep	Overtempt	Reset
CBSS	1	Actual state	Actual state	No change	Actual state	Actual state
CF	0	No change	No change	No change	No change	No change
CFE	0	No change	No change	No change	No change	No change
CFS	0	Actual state	Actual state	Actual state	Actual state	Actual state
CMC	00	No change	No change	No change	No change	No change
CRCC	00000000	No change	No change	No change	No change	No change
CTS	0	0	Actual state	0	0	0
CW	0	No change	No change	No change	No change	No change
CWE	0	No change	No change	No change	No change	No change
ECCS	Actual state	Actual state	Actual state	Actual state	Actual state	Actual state
FNMC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
FNMS	0	Actual state	Actual state	Actual state	Actual state	Actual state
GPMn	0	No change	No change	No change	No change	No change
IDS	See **Table 30**	No change	No change	No change	No change	No change
LKnC	0	No change	No change	No change	No change	No change
MC	100	100	111	001	Don’t care	100
NMS	1	No change	No change	No change	No change	No change
NVMPS	Actual	Actual state	Actual state	Actual state	Actual state	Actual state
NWP	0100	No change	No change	No change	0100	0100
OTW	0	No change	No change	No change	No change	No change
OTWE	0	No change	No change	No change	No change	No change
OTWS	0	Actual state	Actual state	Actual state	Actual state	Actual state
PO	1	No change	No change	No change	No change	No change
RLC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
RSS	00000	No change	No change	No change	10010	Reset source
SDMC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
SDMS	0	Actual state	Actual state	Actual state	Actual state	Actual state
SLPC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
SPIF	0	No change	No change	No change	No change	No change
SPIFE	0	No change	No change	No change	No change	No change
SUPE	0	No change	No change	No change	No change	No change
SYSE	1	No change	No change	No change	No change	No change

Symbol	Off (power-on default)	Standby	Normal	Sleep	Overtempt	Reset
TRXE	0	No change	No change	No change	No change	No change
V1RTC	Defined by V1RTSUC	No change	No change	No change	No change	No change
V1RTSUC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
V1S	0	Actual state	Actual state	Actual state	Actual state	Actual state
V1UE	0	No change	No change	No change	No change	No change
V1U	0	No change	No change	No change	No change	No change
VCS	0	Actual state	Actual state	Actual state	Actual state	Actual state
VEXTC	Defined by VEXTSUC	No change	No change	No change	No change	No change
VEXTSUC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
WDF	0	No change	No change	No change	No change	No change
WDS	0	Actual state	Actual state	Actual state	Actual state	Actual state
WMC	[1]	No change	No change	No change	No change	[1]
WPE	0	No change	No change	No change	No change	No change
WPF	0	No change	No change	No change	No change	No change
WPR	0	No change	No change	No change	No change	No change
WPFE	0	No change	No change	No change	No change	No change
WPRE	0	No change	No change	No change	No change	No change
WPVS	0	No change	No change	No change	No change	No change
WRCNTS	Actual state	Actual state	Actual state	Actual state	Actual state	Actual state

[1] 001 if SDMC = 1; otherwise 010.

STATIC CHARACTERISTICS

T_j=-40°C to +150°C; V_{BAT}=3V to 28V; R_L=$R_{(CANH-CANL)}$=60Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT}=13V; unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Pin BAT						
I_{BAT}	BAT supply current	Normal mode; MC = 111; CAN Active mode				
		CAN recessive; V_{TXD} = V_{V1}		4.3	7.5	mA
		CAN dominant; V_{TXD} = 0 V		43	60	mA
		Sleep mode; MC = 001; CAN Offline mode; V_{BAT} = 7V to 18 V; -40 ºC < T_j < 85 ºC;		30	65	µA
		Standby mode; MC = 100; CAN Offline mode; I_{V1} = 0µA; V_{BAT} = 7 V to 18 V; -40 ºC < T_j < 85 ºC		95	180	µA
		Additional current in CAN Offline Bias mode; -40 ºC < T_j < 85 ºC		25	50	µA
		Input current on WAKE pin WPRE = WPFE = 1； -40 ºC < T_j < 85 ºC		3	6	µA
$V_{th(det)pon}$	Power-on detection threshold voltage	V_{BAT} rising	4.1		4.6	V
$V_{th(det)poff}$	Power-off detection threshold voltage	V_{BAT} falling	2.8		3.3	V
$V_{uvr(CAN)}$	CAN undervoltage recovery voltage	V_{BAT} rising	4.5		5	V
$V_{uvd(CAN)}$	CAN undervoltage detection voltage	V_{BAT} falling	4.2		4.55	V
Pin V1						
V_O	Output voltage	V_{TXD}=V_{V1}; V_{BAT}=5.5V to 28V; I_{V1} = -150mA to 0mA	4.9	5	5.1	V
		V_{BAT} = 5.5V to 28V; V_{TXD} = V_{CANH} = 0V; I_{V1} = -100mA to 0mA	4.9	5	5.1	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{ret(RAM)}$	RAM retention voltage difference	Between V_{BAT} and V_{V1}				
		V_{BAT} = 2V to 3V; I_{V1} = -2mA			100	mV
		V_{BAT} = 2V to 3V; I_{V1}= -200µA			10	mV
V_{drop}	Difference between V_{BAT} and V_{V1}	I_{V1} = -150 mA			600	mV
V_{uvd}	Undervoltage detection voltage	$V_{uvd(nom)}$ = 90%	4.5		4.75	V
		$V_{uvd(nom)}$ = 80%	4		4.25	V
		$V_{uvd(nom)}$ = 70%	3.5		3.75	V
		$V_{uvd(nom)}$ = 60%	3		3.25	V
V_{uvr}	Undervoltage recovery voltage		4.5		4.75	V
$I_{O(sc)}$	Short-circuit output current		-500		-150	mA
$I_{DD(CAN)intV1}$	Internal CAN supply current from V1	Normal mode; MC = 111; CAN Active mode; CAN dominant; TXD=0V; Short-circuit on bus lines; -3V< (V_{CANH} = V_{CANL})< +18V			95	mA
Pin INH						
V_O	output voltage	I_{INH} = -180µA	V_{BAT}-0.8	-	V_{BAT}	V
R_{pd}	pull-down resistance	Sleep mode	1.5	3.5	5	MΩ
Pins SDI/SCK/SCSN						
$V_{th(sw)}$	Switching threshold voltage		0.25V_{V1}		0.75V_{V1}	V
$V_{th(sw)hys}$	Switching threshold voltage hysteresis		0.05V_{V1}			V
$R_{pd(SCK)}$	Pull-down resistance on pin SCK		40	60	80	kΩ
$R_{pu(SCSN)}$	Pull-up resistance on pin SCSN		40	60	80	kΩ
$R_{pd(SDI)}$	Pull-down resistance on pin SDI	SDI < $V_{th(sw)}$	40	60	80	kΩ
$R_{pu(SDI)}$	Pull-up resistance on pin SDI	SDI > $V_{th(sw)}$	40	60	80	kΩ
Pin SDO						
V_{OH}	HIGH-level output volatge	I_{OH} = -4 mA	V_{V1}-0.4			V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OL}	LOW-level output volatge	I_{OL} = 4 mA			0.4	V
$I_{LO(off)}$	Off-state output leakage current	SCSN = V_{V1}; SDO = 0 V or V_{V1}	-5		5	µA
Pin TXD						
$V_{th(sw)}$	Switching threshold voltage		0.25 V_{V1}		0.75 V_{V1}	V
$V_{th(sw)hys}$	Switching threshold voltage hysteresis		0.05 V_{V1}			V
R_{pu}	Pull-up resistance		40	60	80	kΩ
Pin RXD						
V_{OH}	HIGH-level output voltage	I_{OH} = -4mA	V_{V1}-0.4			V
V_{OL}	LOW-level output voltage	I_{OL} = 4mA			0.4	V
R_{pu}	Pull-up resistance	CAN Offline mode	40	60	80	kΩ
Pin WAKE						
$V_{th(sw)r}$	Rising switching threshold voltage		2.8		4.1	V
$V_{th(sw)f}$	Falling switching threshold voltage		2.4		3.75	V
$V_{hys(i)}$	Input hysteresis voltage		250		800	mV
I_i	Input current				1.5	µA
Pins CANH/CANL						
$V_{O(dom)}$	Dominant output voltage	CAN Active mode; TXD = 0V				
		Pin CANH; R_L=50Ω to 65Ω	2.75	3.5	4.5	V
		Pin CANL; R_L=50Ω to 65Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ =V_{CAN} - V_{CANH} - V_{CANL}; V_{CAN} = 5V	-400		400	mV
V_{TXsym}	Transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}; f_{TXD} = 250kHz, 1MHz or 2.5MHz; C_{SPLIT} = 4.7nF; V_{CAN} = 4.75V to 5.25V	0.9V_{CAN}		1.1V_{CAN}	V
$V_{O(dif)}$	Differential output voltage	CAN Active mode (dominant); TXD=0V; V_{CAN}=4.75V to 5.5V				
		R_L = 50 Ω to 65Ω	1.5		3	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
		R_L = 45 Ω to 70Ω	1.4		3.3	V
		R_L = 2240Ω	1.5		5	V
		Recessive; R_L = no load				
		CAN Active / Listen only / Offline bias mode; TXD = V_{VI}	-50		50	mV
		CAN Offline mode	-0.2		0.2	V
$V_{O(rec)}$	Recessive output voltage	CAN Active mode; TXD = V_{VI}; R_L = no load	2	0.5V_{VI}	3	V
		CAN Offline mode; R_L=no load	-0.1	0	0.1	V
		CAN Listen only/Offline bias mode; R_L= no load	2	2.5	3	V
$I_{O(sc)dom}$	Dominant short-circuit output current	CAN Active mode; TXD = 0 V; V_I = 5 V				
		Pin CANH; -3V<V_{CANH}<+27V	-115			mA
		Pin CANL; 15V<V_{CANL}<+18V			115	mA
$I_{O(sc)rec}$	Recessive short-circuit output current	V_{CANL}=V_{CANH} = -27 V to +32 V; TXD = V_{VI}	-3		3	mA
$V_{th(RX)dif}$	Differential receiver threshold voltage	-12 V < V_{CANL} < +12 V; -12 V < V_{CANH} < +12 V				
		CAN Active / Listen only mode	0.5	0.7	0.9	V
		CAN Offline mode	0.4	0.7	1.15	V
$V_{rec(RX)}$	Receiver recessive voltage	-12 V < V_{CANL} < +12 V; -12 V < V_{CANH} < +12 V				
		CAN Active/Listen only mode	-4 [1]		0.5	V
		CAN Offline/Offline bias mode	-4 [1]		0.4	V
$V_{dom(RX)}$	Receiver dominant voltage	-12 V < V_{CANL} < +12 V; -12 V < V_{CANH} < +12 V				
		CAN Active/Listen only mode	0.9		9 [1]	V
		CAN Offline/Offline bias mode	1.15		9 [1]	V
$V_{th(RX)dif(hys)}$	Differential receiver threshold voltage hysteresis	CAN Active / Listen only mode; -12 V < V_{CANL} < +12 V; -12 V < V_{CANH} < +12 V	70	130	200	mV
R_i	Input resistance	-2 V < V_{CANL} < +7 V; -2 V < V_{CANH} < +7 V	30	40	50	kΩ
ΔR_i	Input resistance deviation	0 V < V_{CANL} < +5 V; 0 V < V_{CANH} < +5 V	-1		1	%

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$R_{i(dif)}$	Differential input resistance	-2 V < V_{CANL} < +7 V; -2 V < V_{CANH} < +7 V	60	80	100	kΩ
$C_{i(cm)}$ [1]	Common-mode input capacitance				40	pF
$C_{i(dif)}$ [1]	Differential input capacitance				20	pF
I_L	Leakage current	V_{BAT}= V_{V1}=0V or V_{BAT}= V_{V1}=shorted to ground via 47kΩ V_{CANH} = V_{CANL} = 5 V	-5		5	μA
$I_{DD(CAN)}$	CAN supply current	CAN Active mode; CAN recessive; TXD = V_{V1}	2.5	4.3	6	mA
		CAN Active mode; CAN dominant; TXD = 0 V; R_L= no load	2.5	4.3	6	mA
Pin RSTN						
V_{OL}	LOW-level output voltage	V_{V1} = 1.0 V to 5.5 V; Pull-up resistor to V1 > 900 Ω	0		0.2 V_{V1}	V
R_{pu}	Pull-up resistance		40	60	80	kΩ
$V_{th(sw)}$	Switching threshold voltage		0.25V_{V1}		0.75 V_{V1}	V
$V_{th(sw)hys}$	Switching threshold voltage hysteresis		0.05 V_{V1}			V
Overtemperature protect						
$T_{th(act)otp}$ [1]	Overtemperature protection activation threshold temperature		160	177	195	ºC
$T_{th(rel)otp}$ [1]	Overtemperature protection release threshold temperature		120	137	155	ºC
$T_{th(warn)otp}$ [1]	Overtemperature protection warning threshold temperature		120	137	155	ºC
MTP						
$N_{cy(W)MTP}$	Number of MTP write cycles	V_{BAT} = 6 V to 28 V; T_j = 0 ºC to +125 ºC			500	-

[1] Not tested in production; guaranteed by design.

DYNAMIC CHARACTERISTICS

T_{vj}=-40°C to +150°C; V_{BAT}=3V to 28V; R_L=$R_{(CANH-CANL)}$=60Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT}=13V; unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Pin V1						
$t_{startup}$	Start-up time	From V_{BAT} exceeding the power-on detection threshold 90% undervoltage threshold; C_{V1} = 4.7μF		2.8	4.7	ms
$t_{d(uvd)}$	Undervoltage detection delay time	V1 falling		1		ms
$t_{d(uvd-RSTNL)}$	Delay time from undervoltage detection to RSTN LOW	Undervoltage on V1			63	μs
Pins SCSN/SCK/SDI/SDO						
$t_{cy(clk)}$	Clock cycle time		250			ns
$t_{SPILEAD}$	SPI enable lead time		50			ns
t_{SPILAG}	SPI enable lag time		50			ns
$t_{clk(H)}$	Clock HIGH time		100			ns
$t_{clk(L)}$	Clock LOW time		100			ns
$t_{su(D)}$	Data input set-up time		50			ns
$t_{h(D)}$	Data input hold time		50			ns
$t_{v(Q)}$	Data output valid time	Pin SDO; C_L = 20 pF			50	ns
$t_{d(SDI-SDO)}$	SDI to SDO delay time	SPI address bits and read-only bit; C_L = 20 pF			50	ns
$t_{WH(S)}$	Chip select pulse width HIGH	Pin SCSN	2			μs
$t_{d(SCKL-SCSNL)}$	Delay time from SCK LOW to SCSN LOW		50			ns
Pins CANH/CANL/TXD/RXD						
$t_{d(TXD-busdom)}$	Delay time from TXD to bus dominant				80	ns
$t_{d(TXD-busrec)}$	Delay time from TXD to bus recessive			45		ns
$t_{d(busdom-RXD)}$	Delay time from bus dominant to RXD			45		ns
$t_{d(busrec-RXD)}$	Delay time from Bus recessive to RXD			60		ns

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{d(TXDL-RXDL)}$	Delay time from TXD LOW to RXD LOW	$t_{bit(TXD)}$=200ns		60	255	ns
$t_{d(TXDH-RXDH)}$	Delay time from TXD HIGH to RXD HIGH	$t_{bit(TXD)}$=200ns			255	ns
$t_{bit(bus)}$	Transmitted recessive bit width	$t_{bit(TXD)}$=500ns	435		530	ns
		$t_{bit(TXD)}$=200 ns	155		210	ns
$t_{bit(RXD)}$	Bit time on pin RXD	$t_{bit(TXD)}$=500 ns	400		550	ns
		$t_{bit(TXD)}$=200 ns	120		220	ns
Δt_{rec}	Receiver timing symmetry	$t_{bit(TXD)}$=500 ns	-65		40	ns
		$t_{bit(TXD)}$=200 ns	-45		15	ns
$t_{wake(busdom)}$	Bus dominant wake-up time	First pulse (after first recessive) for wake-up on pins CANH and CANL; CAN Offline mode	0.5		1.8	µs
		Second pulse for wake-up on CANH and CANL	0.5		1.8	µs
$t_{wake(busrec)}$	Bus recessive wake-up time	First pulse for wake-up on pins CANH and CANL; CAN Offline mode	0.5		1.8	µs
		Second pulse (after first dominant) for wake-up on pins CANH and CANL	0.5		1.8	µs
$t_{to(wake)bus}$	Bus wake-up time-out time	Between first and second dominant pulses; CAN Offline mode	0.8		10	ms
$t_{to(dom)TXD}$	TXD dominant time-out time	CAN Active mode; TXD=0V	2.7		3.3	ms
$t_{to(silence)}$	Bus silence time-out time	Recessive time measurement started in all CAN modes	0.95		1.17	s
$t_{d(busact-bias)}$	Delay time from bus Active to Bias				200	µs
$t_{startup(CAN)}$	CAN start-up time	to CTS = 1; when switching to Active mode			220	µs
Watchdog						
$t_{trig(wd)1}$	Watchdog trigger time 1	Normal mode; watchdog Window mode only	0.45*NWP		0.55*NWP	ms
$t_{trig(wd)2}$	Watchdog trigger time 2	Normal/Standby mode	0.9*NWP		1.11*NWP	ms
$t_{d(SCSNH-RSTNL)}$[1]	Delay time from SCSN HIGH to RSTN LOW	Rising edge to falling edge; watchdog in window mode,			0.2	ms

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
		triggered in the first half of the watchdog period (before $t_{trig(wd)1}$)				
Pin RSTN						
$t_{w(rst)}$	Reset pulse width	Output pulse width				
		RLC=00	20		25	ms
		RLC=01	10		12.5	ms
		RLC=10	3.6		5	ms
		RLC=11	1		1.5	ms
		Input pulse width	18			µs
Pin WAKE						
t_{wake}	Wake-up time		50			µs
MTP						
$t_{d(MTPNV)}$	MTPNV delay time	Before factory presets are restored; V_{BAT} = 6 V to 28 V	0.9		1.1	s
$t_{ret(data)}$	Data retention time	T_j=150 ºC	10			year
$t_{prog(MTPNV)}$	MTPNV programming time	Correct CRC code received at address 075h; V_{BAT} = 6V to 28V	10	12	14	ms
Mode Transitions						
$t_{d(act)norm}$	Normal mode activation delay time	MC=111; Delay before CAN is activated after the SBC switches to Normal mode			320	µs

[1] Not tested in production; guaranteed by design.

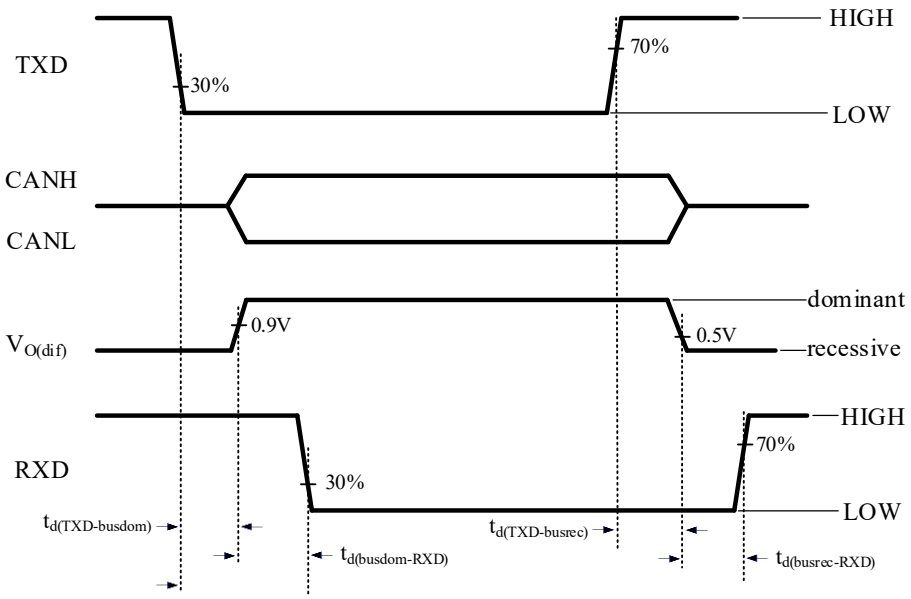


Figure 10 CAN transceiver timing diagram

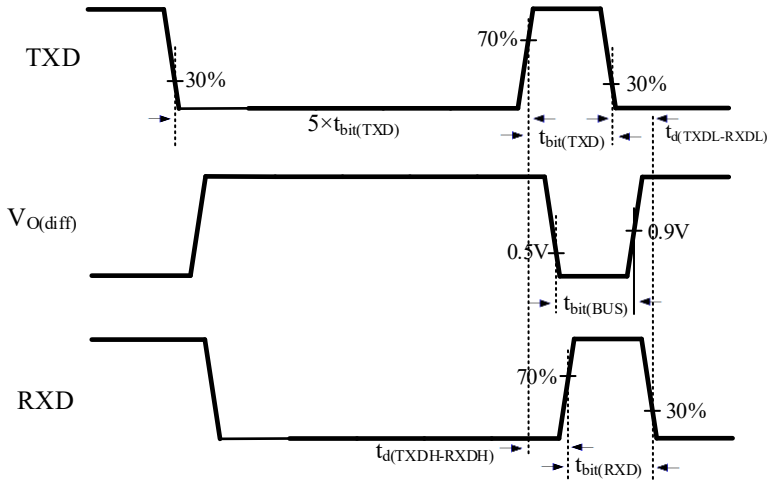
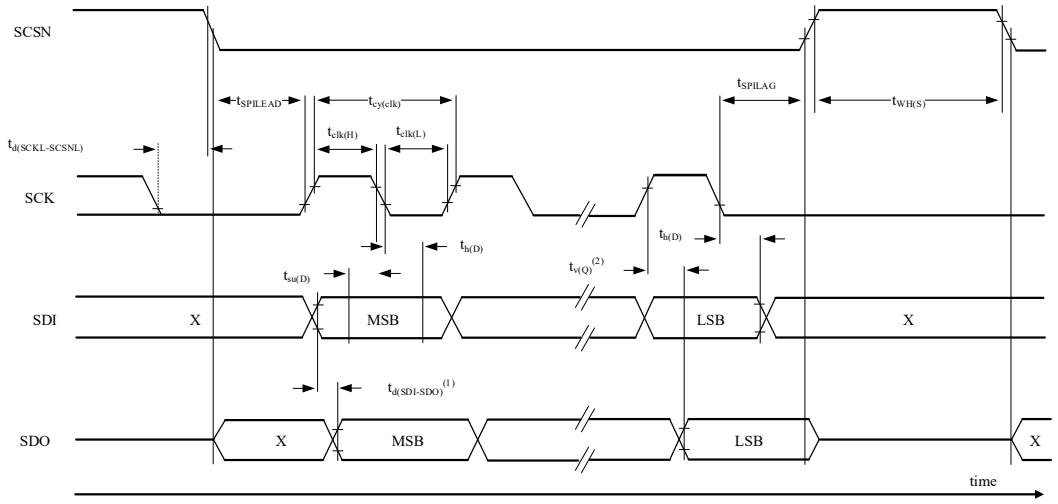


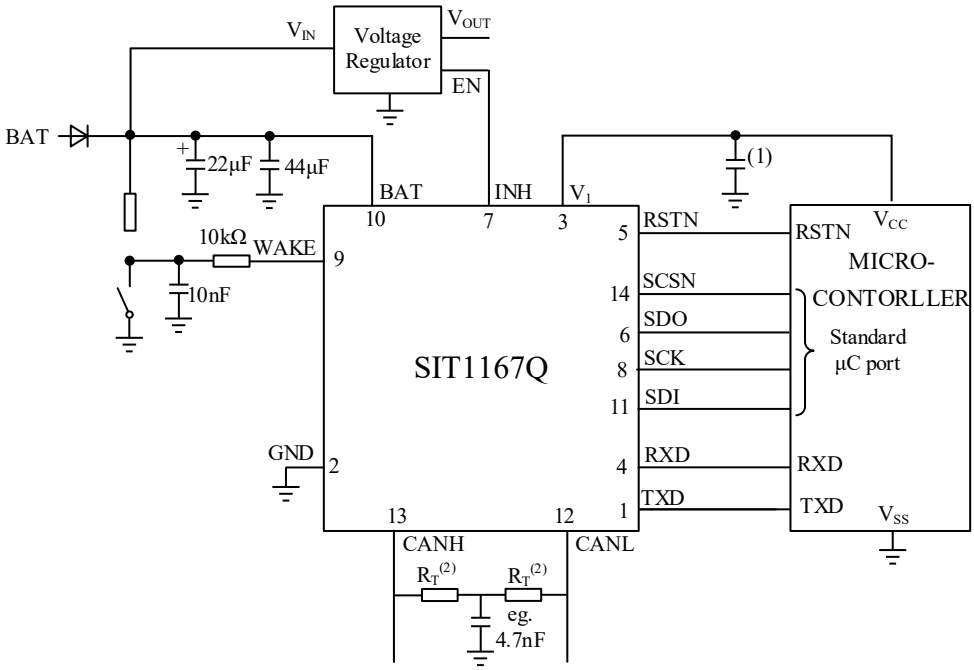
Figure 11 CAN FD timing definitions according to ISO 11898-2:2016



（1）The SDI-to-SDO delay time is valid for SPI address bits and the read-only bit.
（2）The data output valid time is valid for the SPI data bits.

Figure 12 SPI timing diagram

APPLICATION INFORMATION



(1) Actual capacitance value must be a least 1.76μF with 5V DC offset (recommended capacitor value is 6.8μF.
(2) For bus line end nodes, R_T=60Ω in order to support the "split termination concept".

Figure 13 SIT1167Q Typical Application Diagram

Further information on the application of the SIT1167Q can be found in the SIT application hints document.

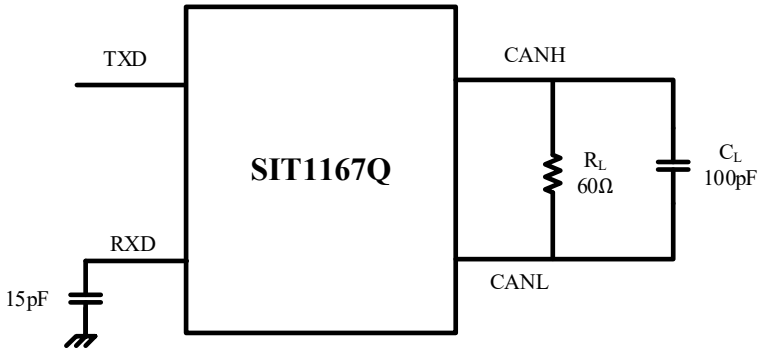


Figure 14 Timing test circuit for CAN transceiver

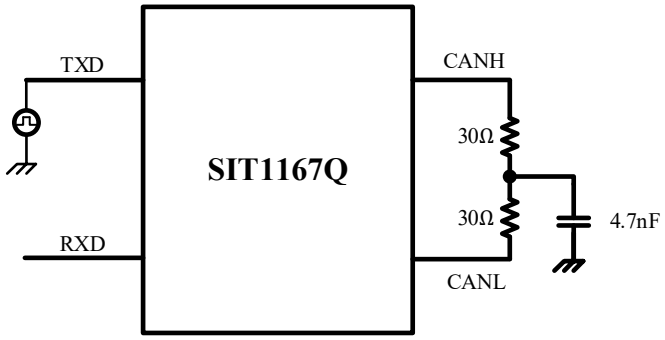
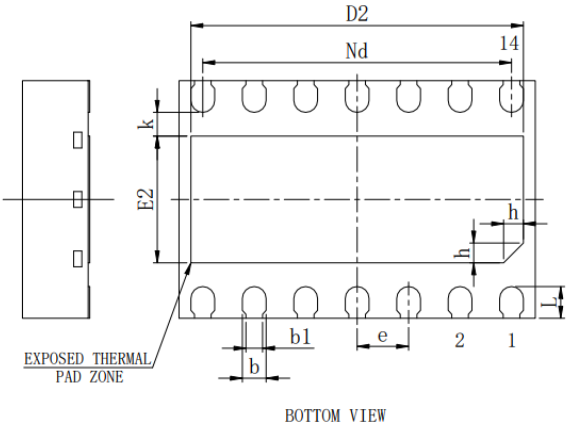


Figure 15 Test circuit for measuring transceiver driver symmetry

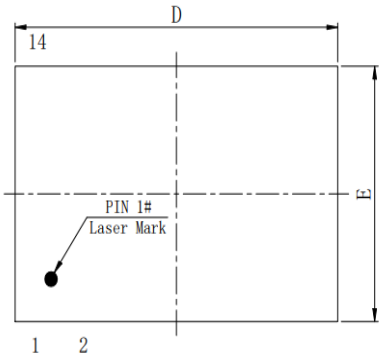
DFN4.5*3-14 DIMENSIONS

Package size

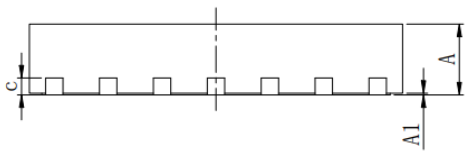
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
b1		0.21REF	
c		0.203REF	
D	4.40	4.50	4.60
D2	4.10	4.20	4.30
e		0.65BSC	
Nd		3.90BSC	
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
L	0.35	0.40	0.45
h	0.20	0.25	0.30
K		0.30REF	



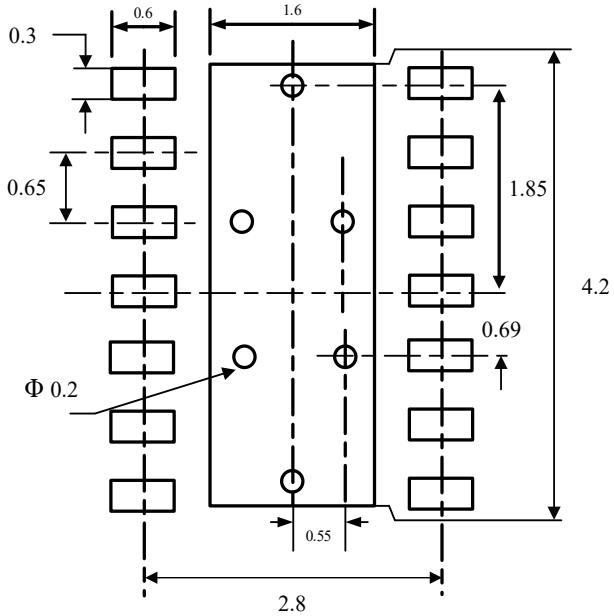
BOTTOM VIEW



TOP VIEW

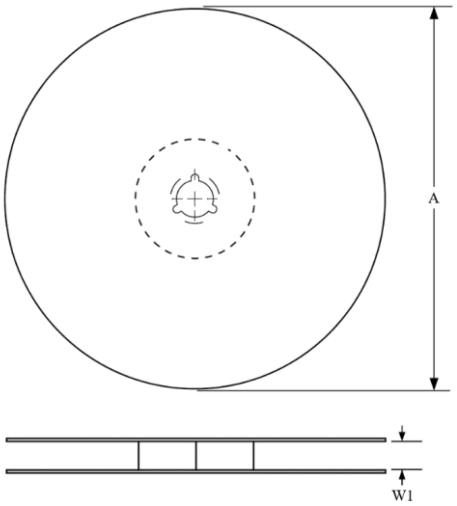


SIDE VIEW

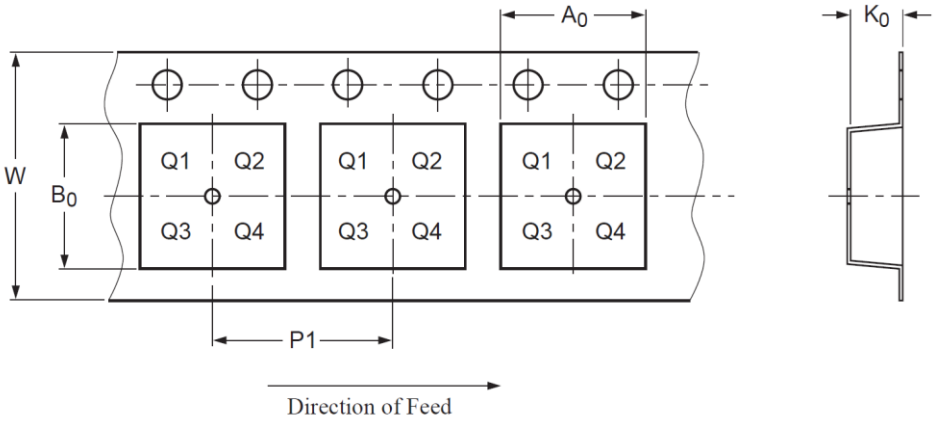


LAND PATTERN EXAMPLE (Unit: mm)

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

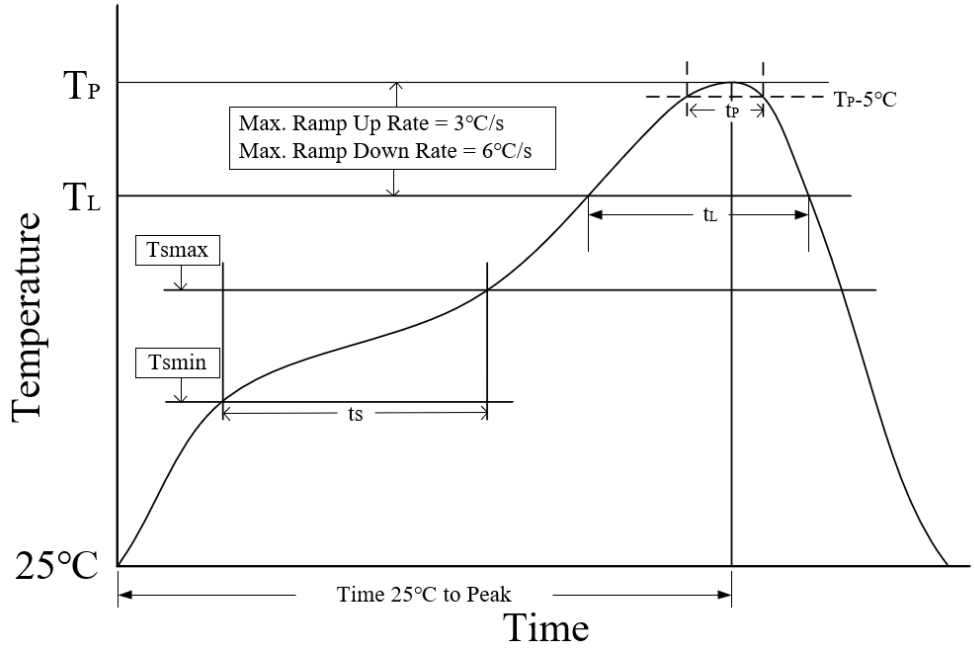
Package Type	Reel Diameter A (mm)	Tape Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
DFN4.5×3-14	329±1	12.4	3.75±0.1	4.25±0.1	1.00±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	MSL	PACKING
SIT1167QTK	DFN4.5×3-14	MSL3	Tape and reel

Leadless DFN4.5×3-14 is packed with 3000 pieces/disc in braided packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5 °C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Datasheet status	Revision date
V1.0	Initial version	October 2025