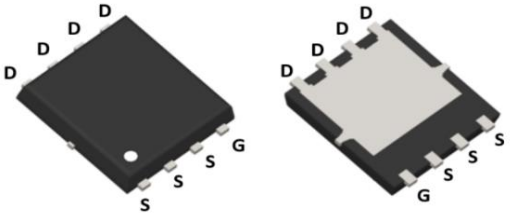
SNM035R4DRA

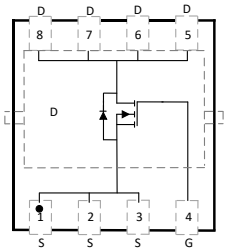
Single N-Channel, 30V, 36A, Power MOSFET

http://www.sitcores.com/

V_{DS} (V)	Max. $R_{DS(on)}$ (mΩ)
30	5.4 @V_{GS}=10V
	9.1 @V_{GS}=4.5V



PDFN3.3X3.3-8L



Internal schematic diagram

Description

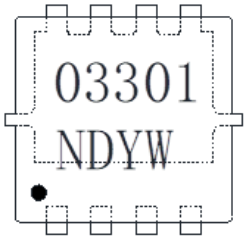
The SNM035R4DRA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced Split Gate Trench and design to provide excellent RDS(ON) with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM035R4DRA is Pb-free.

Features

- Split Gate Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Package PDFN3.3X3.3-8L

Applications

- DC/DC converters
- CPU, GPU, Charger Switching MOS
- Power supply converters circuit



03301 = Device Code
ND = Special Code
Y = Year
W = Week(A~z)

Marking

Order information

Device	Package	Shipping
SNM035R4DRA-8/TR	PDFN3333-8L	5000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current [e]	T_C=25°C	I_D	36	A
	T_C=100°C		34	A
Pulsed Drain Current [c]		I_{DM}	144	A
Continuous Drain Current	T_A=25°C	I_{DSM}	22	A
	T_A=70°C		18	
Avalanche Energy L=0.3mH		E_{AS}	36	mJ
Power Dissipation [b]	T_C=25°C	P_D	23	W
	T_C=100°C		9	
Power Dissipation [a]	T_A=25°C	P_{DSM}	3.9	W
	T_A=70°C		2.5	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	24.7	32.1	°C/W
	Steady State		50.4	63.0	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	4.4	5.4	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm^2 area). The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150°C. The value is only for reference, any application depends on the user's specific board design.

b The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

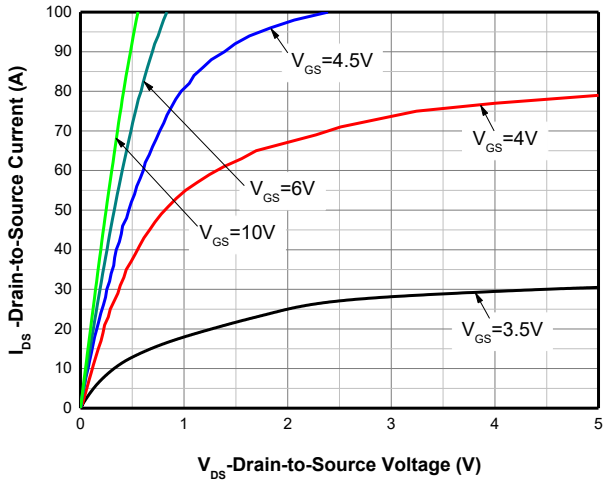
d The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

e The maximum current rating by source bonding technology.

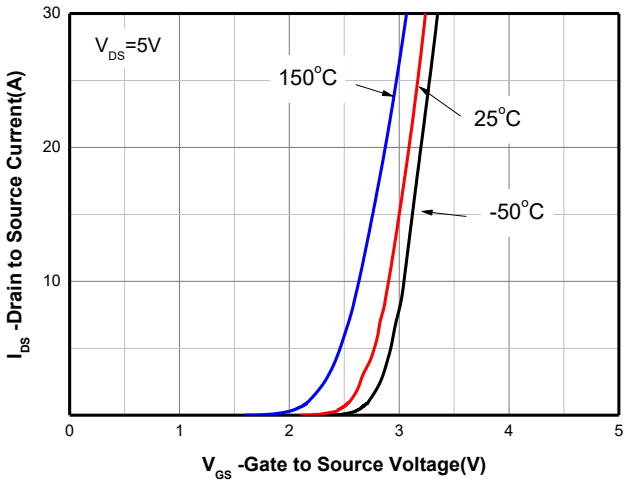
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =30V, V_{GS} = 0V			1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	1.3	1.8	2.5	V
Drain-to-source On-resistance	$R_{DS(on)}$	V_{GS} =10V, I_D = 18A		4.3	5.4	mΩ
		V_{GS} = 4.5V, I_D=18A		6.7	9.1	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS}= 0 V, f = 1.0MHz, V_{DS}= 15 V		991		pF
Output Capacitance	C_{OSS}			443		
Reverse Transfer Capacitance	C_{RSS}			21		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS}= 10V, V_{DD}= 15 V, I_D=18 A		16.7		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS}= 4.5V, V_{DD}= 15V, I_D =18 A		7.8		
Gate-to-Source Charge	Q_{GS}	V_{GS}= 10V, V_{DD}= 15 V, I_D =18 A		3.7		
Gate-to-Drain Charge	Q_{GD}			1.4		
Gate Resistance	R_g	f=1MHz		2.1		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS}= 10V, V_{DD}= 15 V, I_D =18A, R_G=3Ω		5.0		ns
Rise Time	tr			44.9		
Turn-Off Delay Time	td(OFF)			12.9		
Fall Time	tf			2.6		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1A		0.72	1.2	V
Reverse Recovery Time	trr	I_F=18A, di/dt=100A/us		16.3		nS
Reverse Recovery Charge	Qrr			5.3		nC

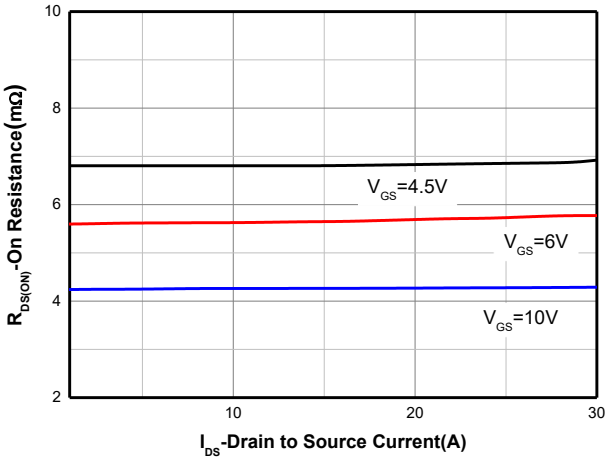
Typical Characteristics (Ta=25°C, unless otherwise noted)



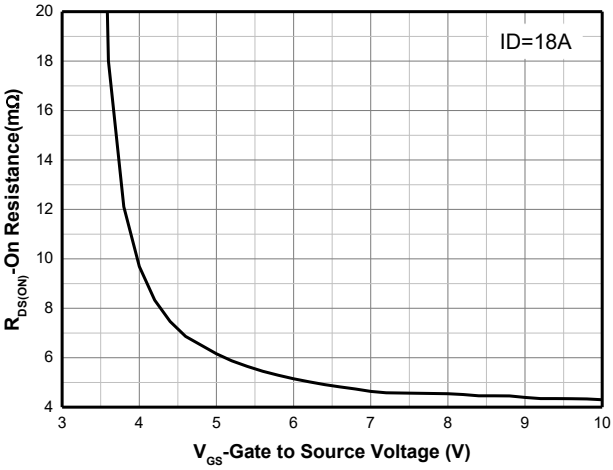
Output Characteristics [d]



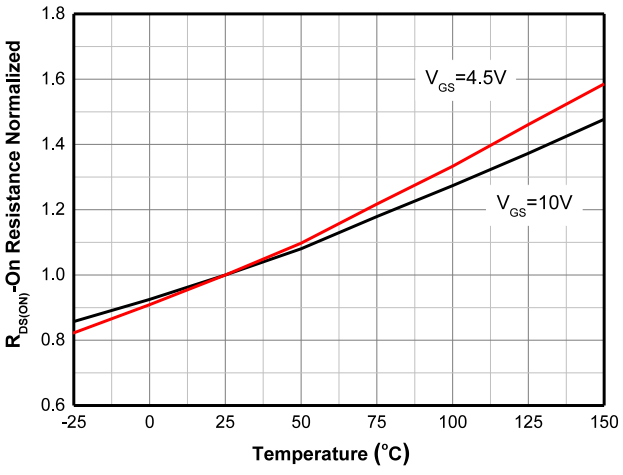
Transfer Characteristics [d]



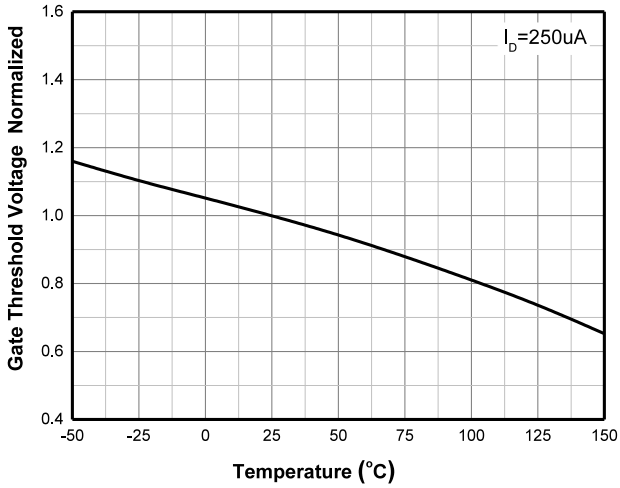
On-Resistance vs. Drain Current [d]



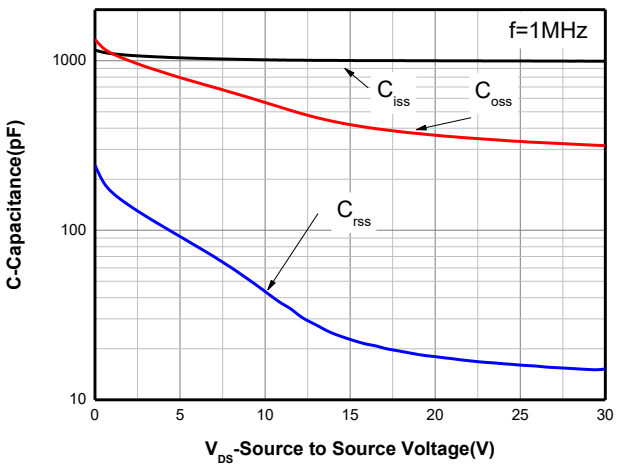
On-Resistance vs. Gate-to-Source Voltage [d]



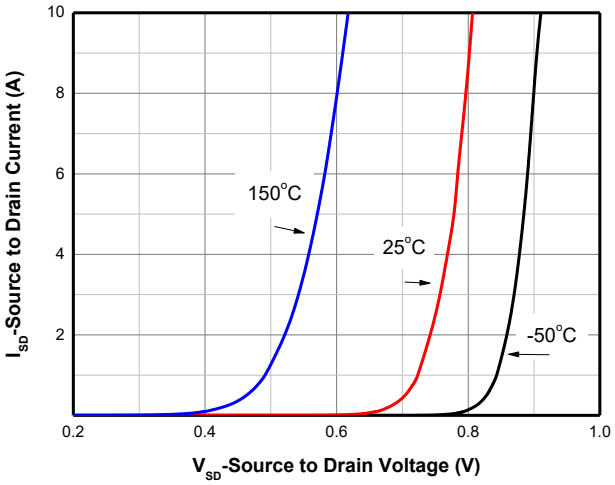
On-Resistance vs. Junction Temperature [d]



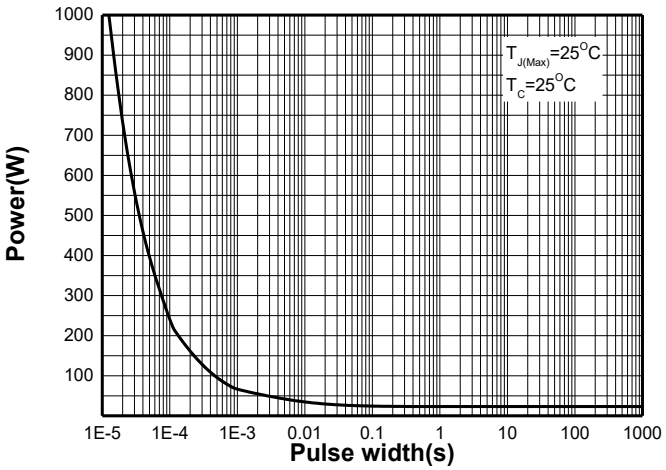
Threshold Voltage vs. Temperature



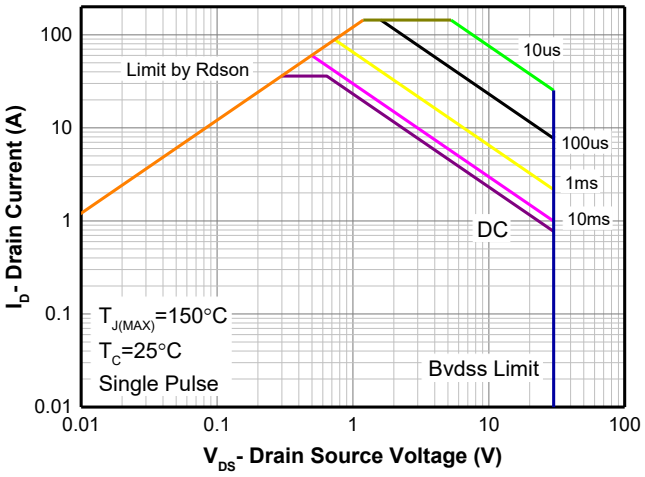
Capacitance



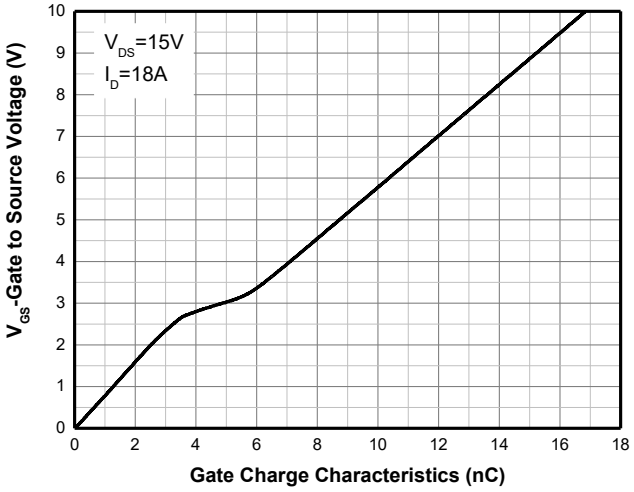
Body Diode Forward Voltage [d]



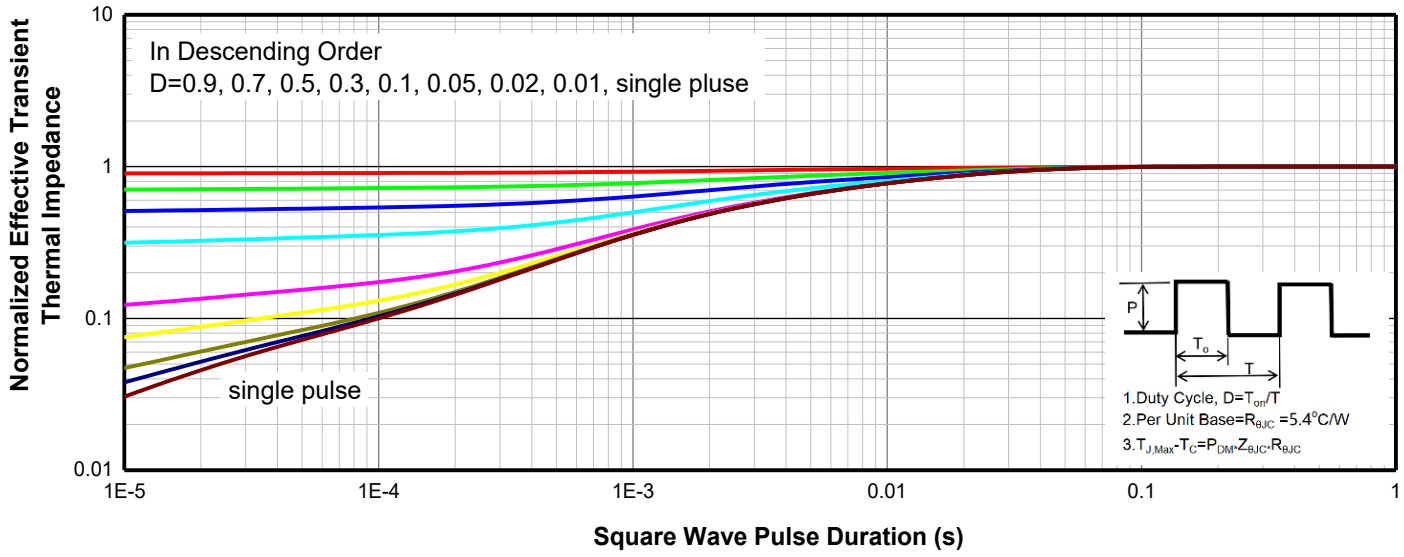
Single Pulse power



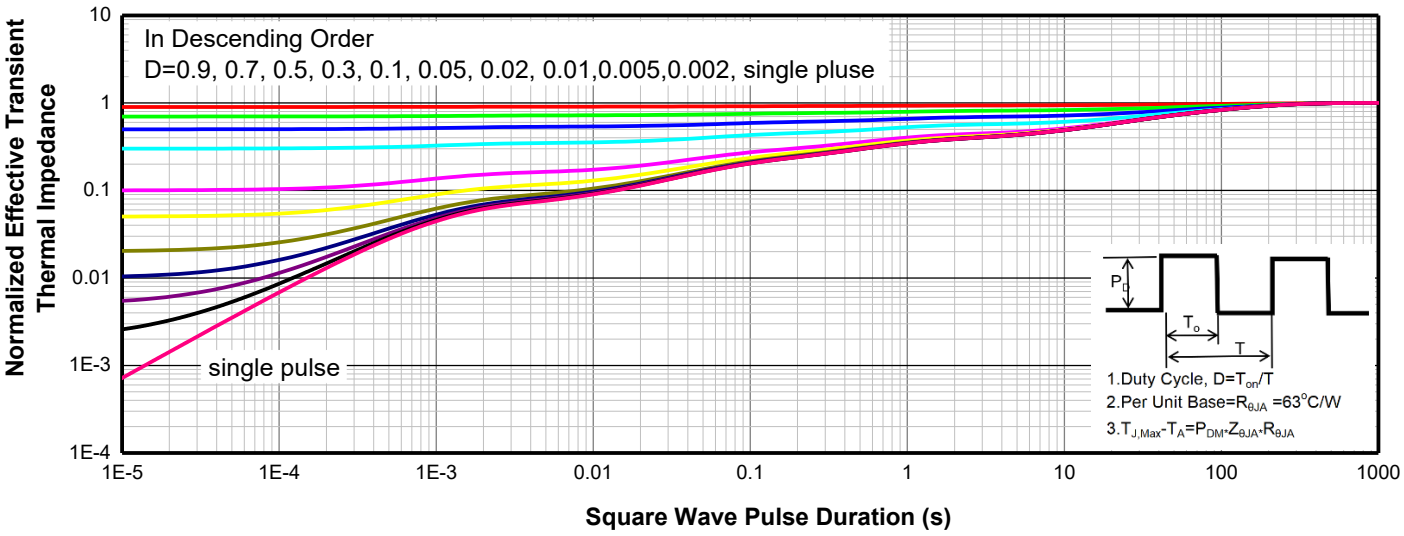
Safe Operating Area



Gate Charge Characteristics



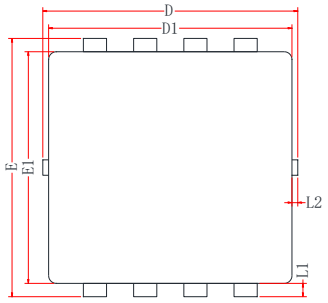
Transient Thermal Response (Junction-to-Case)



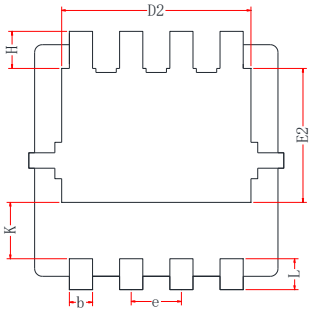
Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

PDFN3333-8L

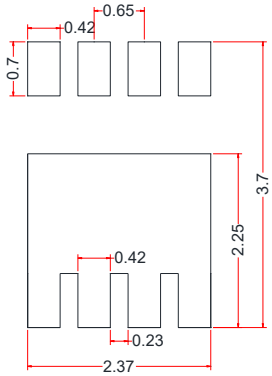


TOP VIEW



BOTTOM VIEW

SIDE VIEW

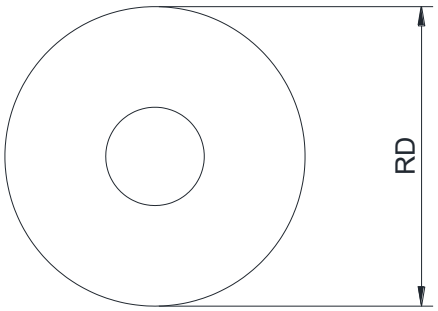


RECOMMENDED LAND PATTERN(Unit:mm)

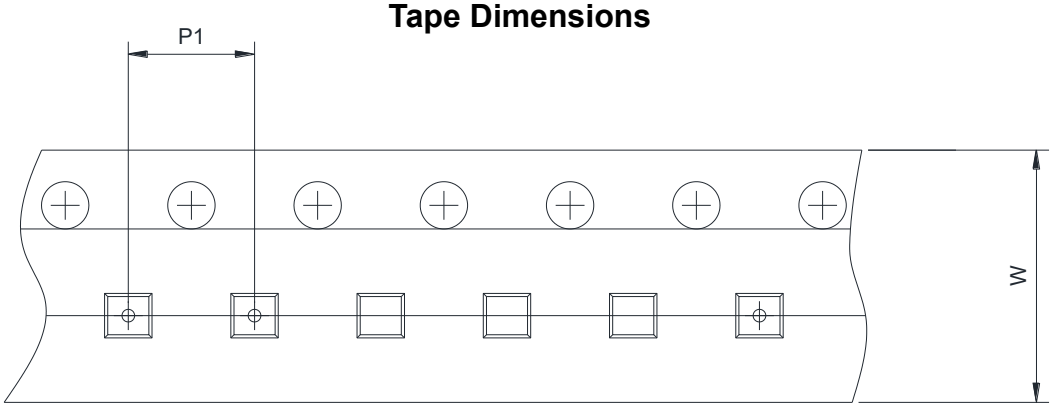
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.35
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.35	2.45	2.55
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.64	1.74	1.84
H	0.32	0.42	0.52
K	0.59	0.69	0.79
L	0.25	0.40	0.55
L1	0.10	0.15	0.20
L2	-	-	0.15
θ	8°	10°	12°

TAPE AND REEL INFORMATION

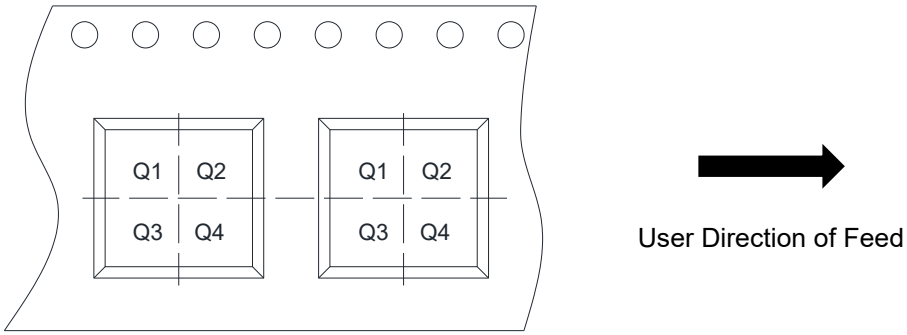
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch	☑ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☑ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☑ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4