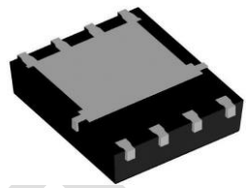
# SNM062R2DNA

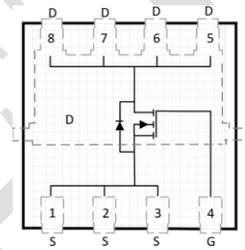
## Single N-Channel, 60V, 187A, Power MOSFET

| $V_{DS}$(V) | Max. $R_{DS(on)}$ (mΩ) |
|---|---|
| 60 | 2.2@$V_{GS}$=10V |

http://www.sitcores.com/



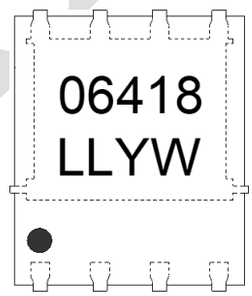
PDFN5X6-8L




Pin configuration (Top view)

## Description

The SNM062R2DNA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced Split Gate technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in high performance DC-DC conversion, power switch and charging circuit. Standard Product SNM062R2DNA is in compliance with RoHS.




06418 = Device Code
LL = Special Code
Y = Year
W = Week

Marking

## Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance
- 100% Rg and Avalanche tested
- MSL3

## Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

## Order information

| Device | Package | Shipping |
|---|---|---|
| SNM062R2DNA-8/TR | PDFN5X6-8L | 5000/Tape&Reel |

## Absolute Maximum ratings ($T_J$=25°C, unless otherwise noted)

| Parameter | | Symbol | Maximum | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 60 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | |
| Continuous Drain Current | $T_C$=25°C | $I_D$ | 187 | A |
| | $T_C$=100°C | | 118 | |
| Pulsed Drain Current[c] | | $I_{DM}$ | 434 | A |
| Continuous Drain Current | $T_A$=25°C | $I_{DSM}$ | 46 | A |
| | $T_A$=70°C | | 36 | |
| Avalanche Energy L=0.3mH | | $E_{AS}$ | 342 | mJ |
| Power Dissipation[b] | $T_C$=25°C | $P_D$ | 132 | W |
| | $T_C$=100°C | | 53 | |
| Power Dissipation[a] | $T_A$=25°C | $P_{DSM}$ | 7.8 | W |
| | $T_A$=70°C | | 5.0 | |
| Operating Junction Temperature | | $T_J$ | -55°C to 150°C | °C |
| Storage Temperature Range | | $T_{STG}$ | -55°C to 150°C | °C |

## Thermal resistance ratings

| Single Operation | | | | | |
|---|---|---|---|---|---|
| Parameter | | Symbol | Typical | Maximum | Unit |
| Junction-to-Ambient Thermal Resistance[a] | t ≤ 10 s | $R_{\theta JA}$ | 13 | 16 | °C/W |
| | Steady State | | 37 | 45 | |
| Junction-to-Case Thermal Resistance[b] | Steady State | $R_{\theta JC}$ | 0.75 | 0.95 | |

**Note:**

a. FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm$^2$ area). The power dissipation $P_D$ is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$≤10s value and the $T_{J(MAX)}$=150°C. The value is only for reference, any application depends on the user's specific board design.

b. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c. Repetitive rating, duty cycle ~1%, keep initial $T_J$ =25°C, the maximum allowed junction temperature of 150°C.

d. The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

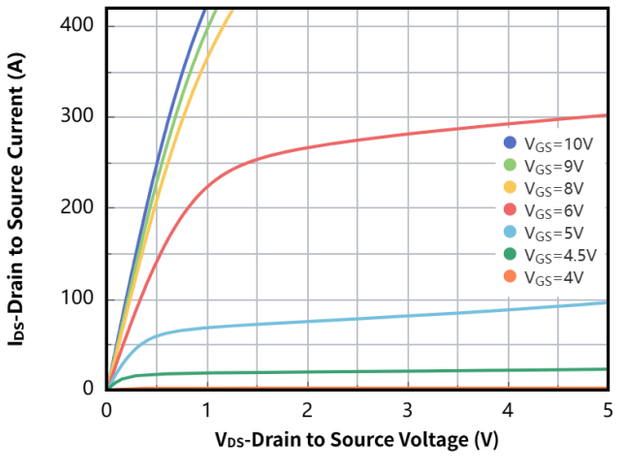
e. The parameter is not subject to production test – verified by design / characterization.

## Electronics Characteristics ($T_J$=25°C, unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain-to-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$= 0 V, $I_D$ = 250uA | 60 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$= 60V, $V_{GS}$= 0V | | | 1 | uA |
| Gate-to-source Leakage Current | $I_{GSS}$ | $V_{DS}$= 0V, $V_{GS}$ = ±20V | | | 100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$= $V_{DS}$, $I_D$= 250uA | 2.5 | 3.0 | 3.5 | V |
| Drain-to-source On-resistanc[d] | $R_{DS(on)}$ | $V_{GS}$= 10V, $I_D$= 30A | | 1.8 | 2.2 | mΩ |
| **CHARGES, CAPACITANCES AND GATE RESISTANCE** | | | | | | |
| Input Capacitance[e] | $C_{ISS}$ | $V_{GS}$= 0V, f= 1.0MHz, $V_{DS}$= 30V | | 4486 | | nF |
| Output Capacitance[e] | $C_{OSS}$ | | | 1714 | | |
| Reverse Transfer Capacitance[e] | $C_{RSS}$ | | | 44 | | |
| Total Gate Charge[e] | $Q_{G(TOT)}$ | $V_{GS}$= 10V, $V_{DD}$= 30V, $I_D$= 30A | | 63.4 | | nC |
| Gate-to-Source Charge[e] | $Q_{GS}$ | $V_{GS}$= 10V, $V_{DD}$= 30V, $I_D$= 30A | | 20.7 | | |
| Gate-to-Drain Charge[e] | $Q_{GD}$ | | | 12.5 | | |
| Gate Resistance | Rg | f= 1MHz | | 2 | | Ω |
| **SWITCHING CHARACTERISTICS[e]** | | | | | | |
| Turn-On Delay Time | td(ON) | $V_{GS}$= 10V,$V_{DD}$= 30V, $I_D$= 30A , $R_G$= 2Ω | | 14 | | ns |
| Rise Time | tr | | | 45 | | |
| Turn-Off Delay TimeTurn-Off Delay Time | td(OFF) | | | 34 | | |
| Fall Time | tf | | | 14 | | |
| **BODY DIODE CHARACTERISTICS** | | | | | | |
| Forward Voltage[d] | $V_{SD}$ | $V_{GS}$= 0V, $I_S$= 30A | | 0.8 | 1.2 | V |
| Maximum Continuous Current[e] | $I_S$ | | | | 125 | A |
| Body Diode Reverse Recovery Time[e] | trr | $I_F$= 30A, dI/dt= 100A/μs | | 62 | | ns |
| Body Diode Reverse Recovery Charge[e] | Qrr | | | 95 | | nC |

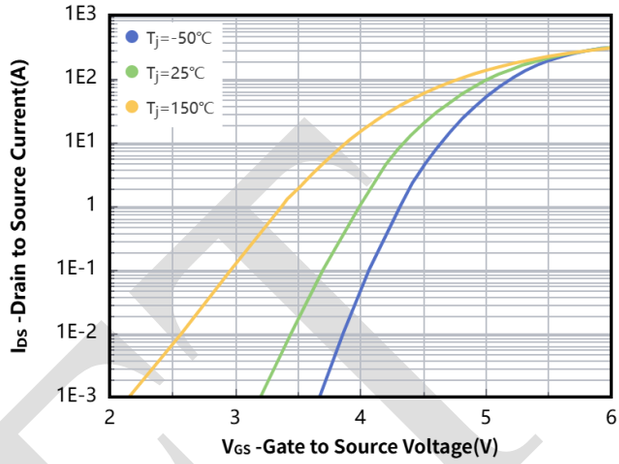
## Typical Characteristics

Tj=25℃



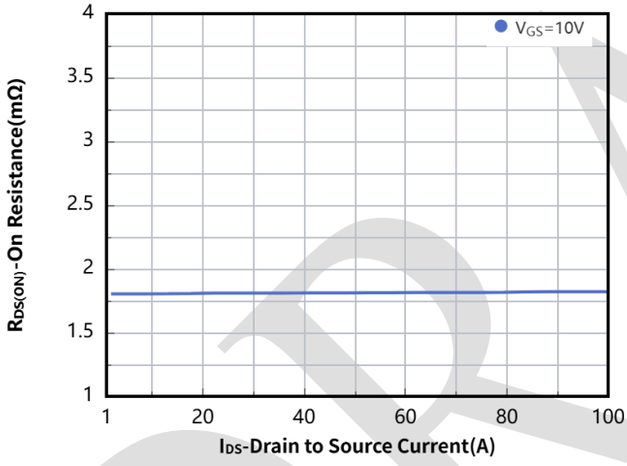

**Output Characteristics** [d]

$V_{DS}$=5V



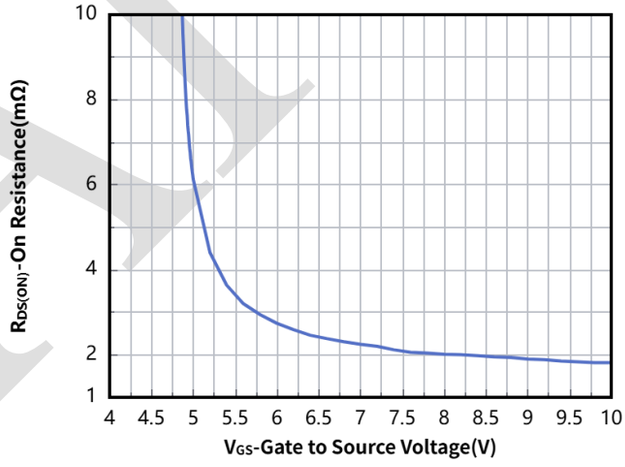

**Transfer Characteristics** [d]

Tj=25℃



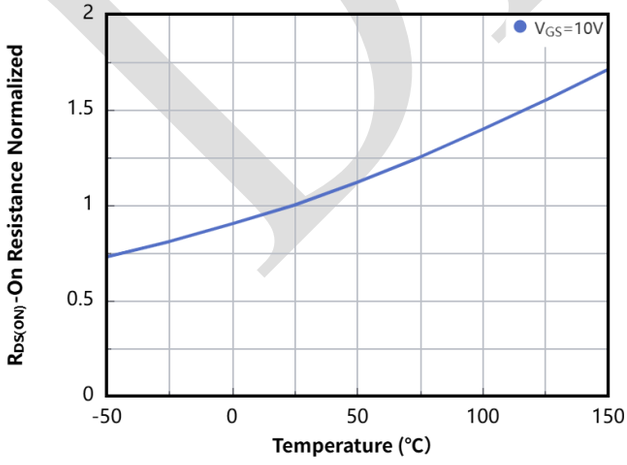

**On-Resistance vs. Drain Current** [d]

Tj= 25℃，$I_D$=30A



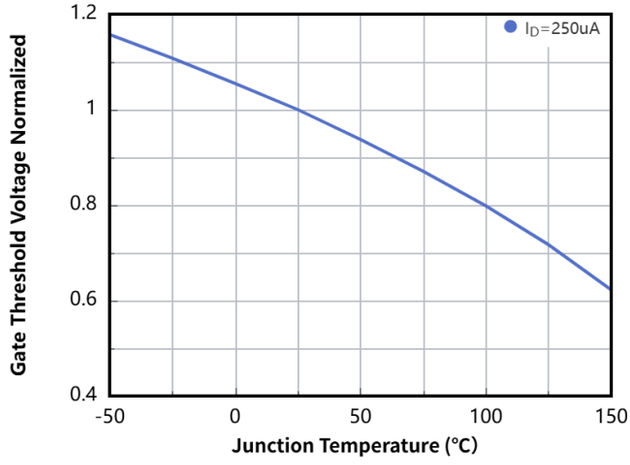

**On-Resistance vs. Gate to Source Voltage**[d]

$V_{GS}$=10V,$I_D$=30A




**On-Resistance vs. Junction Temperature** [d]

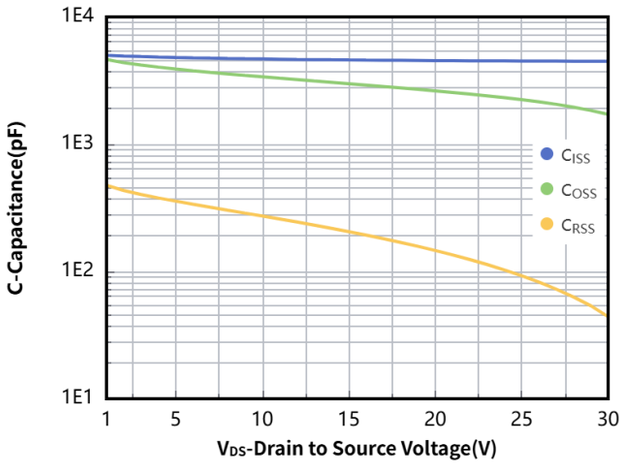
$V_{GS}$=$V_{DS}$




**Threshold Voltage vs. Temperature**

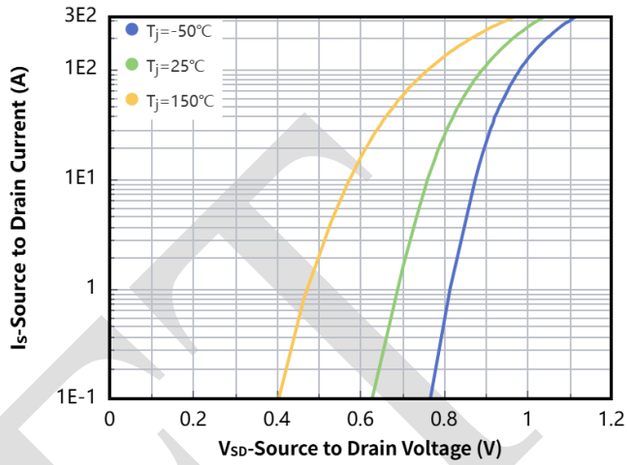
## Typical Characteristics (Ta=25°C, unless otherwise noted)

VGS= 0V, f= 1MHz



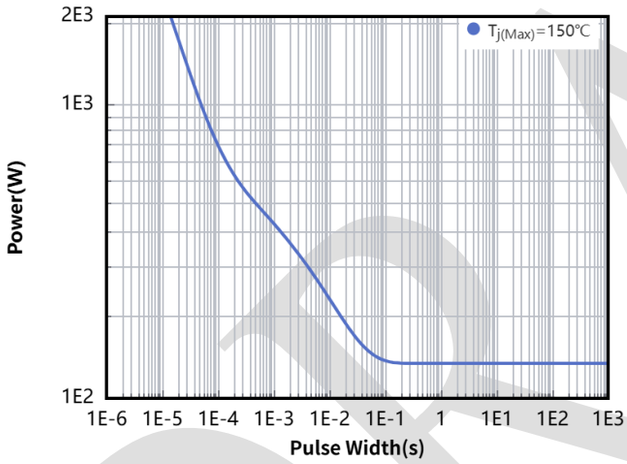

**Capacitance**

VGS= 0V



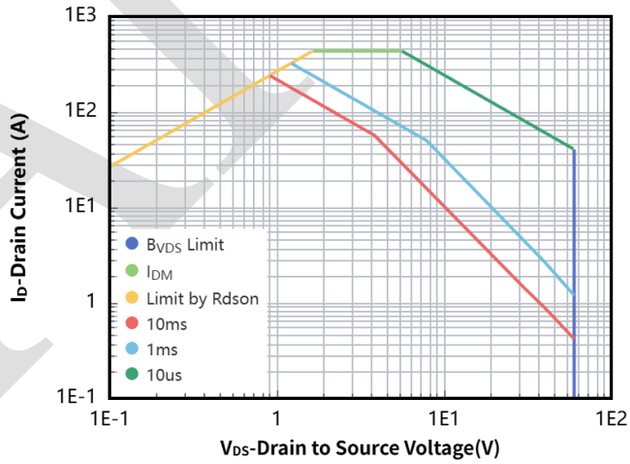

**Body Diode Forward Voltage [d]**

TC= 25℃



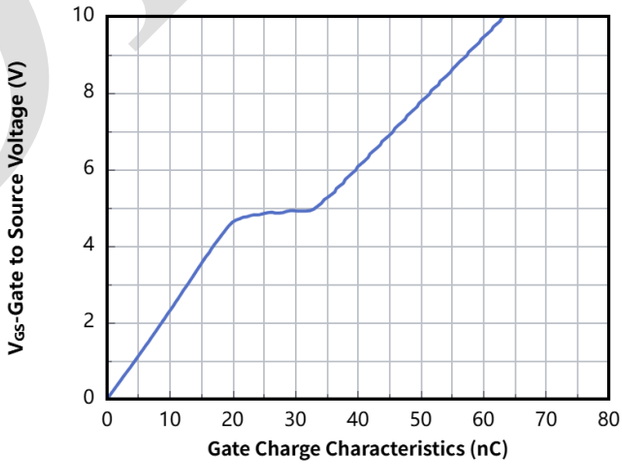

**Single Pulse power**

TJ(MAX)= 150℃,TC= 25℃,Single Pulse

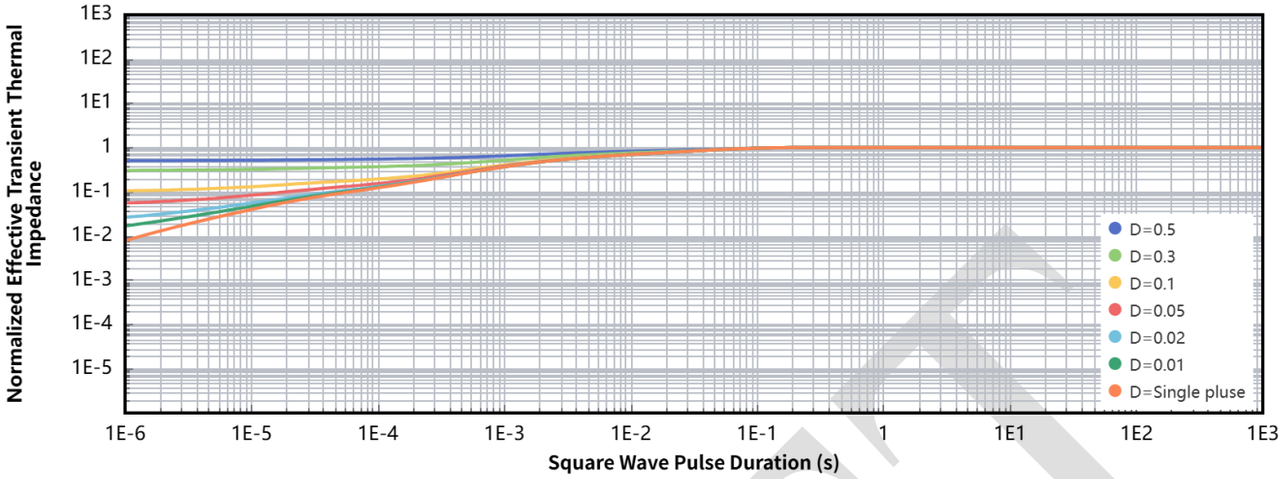


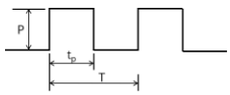

**Safe Operating Area**

Tj= 25℃,ID= 30A



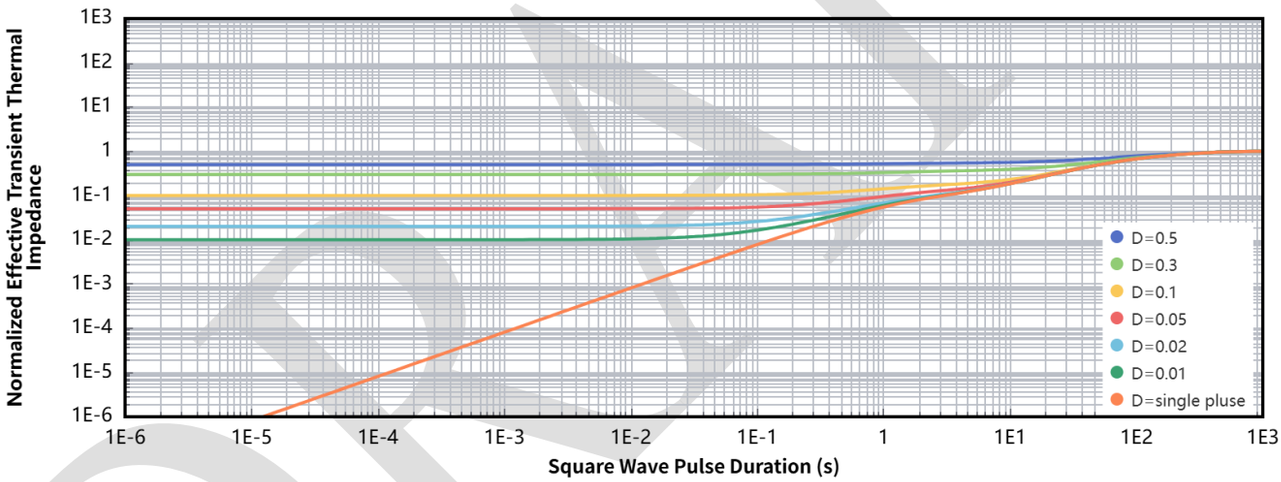

**Gate Charge Characteristics**

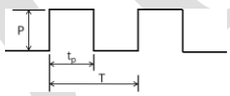



1.Duty Cycle,D=tp/T ;2.Per Unit Base=$R_{\theta JC}$=0.95℃/W ;
3.$T_{J(MAX)}$-$T_C$=$P_{DM}$*$Z_{\theta JC}$*$R_{\theta JC}$

**Transient Thermal Response (Junction-to-Case)**



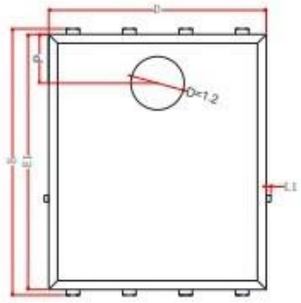



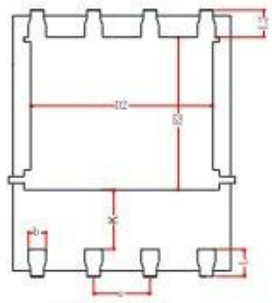

1.Duty Cycle,D=tp/T ; 2.Per Unit Base=$R_{\theta JA}$=45℃/W;
3.$T_{J(MAX)}$-$T_A$=$P_{DM}$*$Z_{\theta JA}$*$R_{\theta JA}$

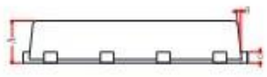
**Transient Thermal Response (Junction-to-Ambient)**

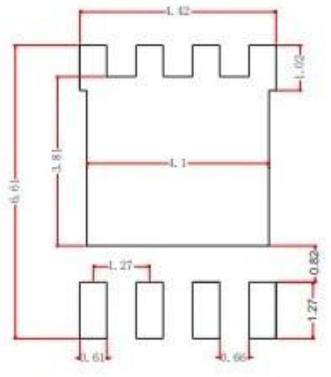
## PACKAGE OUTLINE DIMENSIONS

**PDFN5x6-8L**



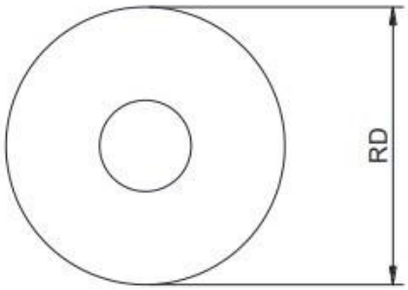



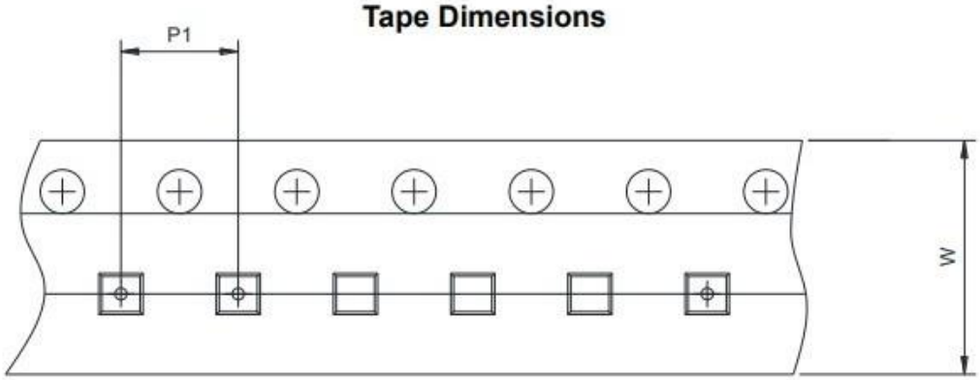

| Symbol | Dimensions in Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.90 | 0.95 | 1.00 |
| b | 0.35 | 0.40 | 0.45 |
| c | 0.21 | 0.25 | 0.34 |
| D | 4.80 | 4.90 | 5.00 |
| D2 | 3.82 | - | 4.11 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 5.75 | 5.80 |
| E2 | 3.18 | - | 3.54 |
| e | 1.27BSC | | |
| K | 1.10 | - | - |
| L | 0.51 | 0.61 | 0.71 |
| L1 | - | - | 0.10 |
| L2 | 0.51 | 0.61 | 0.71 |
| P | 1.00 | 1.10 | 1.20 |
| θ | 8° | - | 12° |

## PACKAGE OUTLINE DIMENSIONS

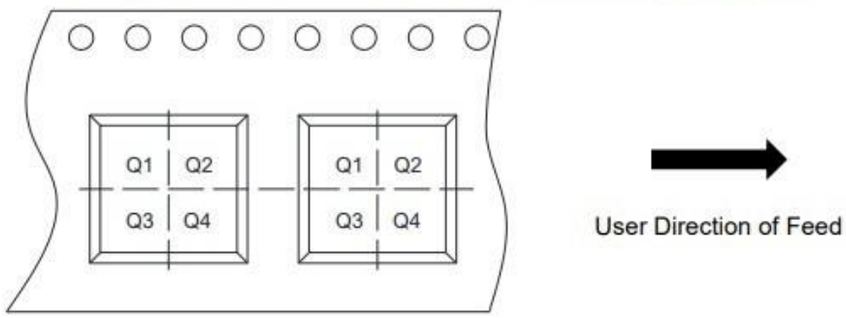
**Reel Dimensions**




**Tape Dimensions**




**Quadrant Assignments For PIN1 Orientation In Tape**




| | | | | | |
|---|---|---|---|---|---|
| RD | Reel Dimension | ☐ 7inch | ☑ 13inch | | |
| W | Overall width of the carrier tape | ☐ 8mm | ☑ 12mm | ☐ 16mm | |
| P1 | Pitch between successive cavity centers | ☐ 2mm | ☐ 4mm | ☑ 8mm | |
| Pin1 | Pin1 Quadrant | ☑ Q1 | ☐ Q2 | ☐ Q3 | ☐ Q4 |